UCC53x0 3kV$_{RMS}$ 隔离式单通道栅极驱动器

1 特性

- 3V 至 15V 输入电源电压
- 13.2V 至 33V 输出驱动器电源电压
- 特性选项
  - 分离输出（UCC5320S 和 UCC5390S）
  - IGBT 发射极采用 UVLO（UCC5320E 和 UCC5390E）
  - 米勒钳位选项（UCC5310M 和 UCC5350M）
- 输入引脚具有负 5V 电压处理能力
- UCC5320S、UCC5320E 和 UCC5310M 具有 60ns 传播延迟（典型值）
- UCC5390S、UCC5390E 和 UCC5350M 具有 65ns 传播延迟（典型值）
- 100kV/µs 最小共模瞬态抗扰度 (CMTI)
- 可承受的隔离浪涌电压：4242V$_{PK}$
- 安全相关认证：
  - 符合 DIN V VDE V 0884-10 和 DIN EN 61010-1 标准的 4242 V$_{PK}$ 隔离（计划）
  - 符合 UL 1577 标准且长达 1 分钟的 3000 V$_{RMS}$ 隔离（计划）
  - CSA 组件验收通知 5A，IEC 60950-1 和 IEC 61010-1 终端设备标准（计划）
  - 符合 GB4943.1-2011 标准的 CQC 认证（计划）
- 针对所有引脚的 4kV ESD
- CMOS 输入
- 8 引脚窄体 SOIC 封装
- 工作温度范围：–40°C 至 +125°C 环境

2 应用

- 工业电机控制驱动
- 工业用电源
- 太阳能逆变器
- 混合动力汽车 (HEV) 和电动车 (EV) 电源模块
- 感应加热

3 说明

UCC53x0 是一系列紧凑型单通道隔离式 IGBT、SiC 和 MOSFET 栅极驱动器，具有出色的隔离等级和型号，适用于引脚排列配置和驱动强度。

UCC53x0 采用 8 引脚 SOIC (D) 封装。该封装具有 4mm 的爬电和余隙，可以支持高达 3kV$_{RMS}$ 的隔离电压，很适合 需要 基本隔离的应用。基于这些各种不同的选项和宽电源范围，UCC53x0 系列十分适合电机驱动和工业电源。

UCC53x0S 选项提供分离输出，可以用于控制驱动器的上升和下降时间。UCC53x0M 选项将晶体管的栅极连接到内部钳位，以防止米勒电流造成假接通。UCC53x0E 选项的 UVLO2 以 GND2 为基准，方便了双极供电。

与光耦合器不同，UCC53x0 系列的部件间偏移更低，传播延迟更小，工作温度更高，并且 CMTI 更大。

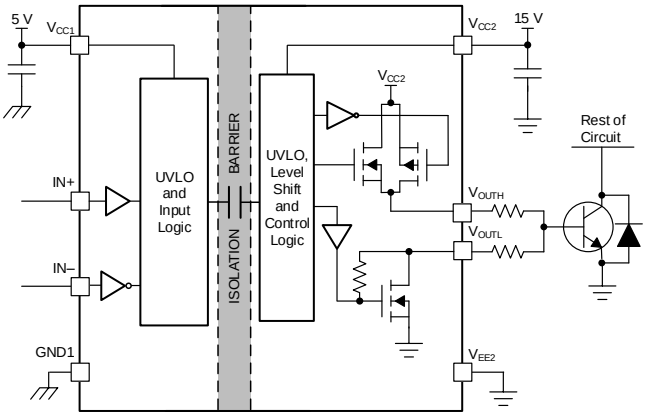
器件信息(1)

器件型号	最低拉电流和灌电流	说明
UCC5310M	2.4A 和 1.1A	米勒钳位
UCC5320S	2.4A 和 2.2A	分离输出
UCC5320E	2.4A 和 2.2A	UVLO 以 IGBT 发射极为基准
UCC5350M	5A 和 5A	米勒钳位
UCC5390S	10A 和 10A	分离输出
UCC5390E	10A 和 10A	UVLO 以 IGBT 发射极为基准

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

(2) 有关器件的详细比较，请参见 *器件比较表*

功能框图（S 版本）



目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (June 2017) to Revision B **Page**

- 已更改 最低环境工作温度为 -55°C 至 -40°C ... 1
- 已添加 将 UCC5350 和 UCC5390 器件添加到了数据表 ... 1

Changes from Original (June 2017) to Revision A **Page**

- 已删除 从标题中删除了可用于未来 10A 器件的 17A 规格 ... 1

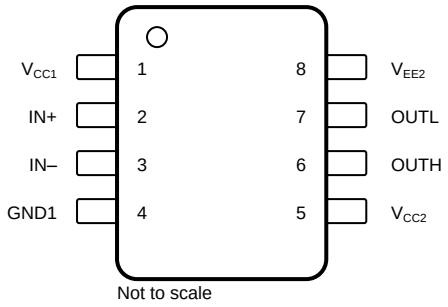
5 Device Comparison Table

DEVICE OPTION(1)	MINIMUM SOURCE CURRENT	MINIMUM SINK CURRENT	PIN CONFIGURATION	ISOLATION RATING(2)
UCC5310M	2.4 A	1.1 A	Miller clamp	3 kV_{RMS}
UCC5320E	2.4 A	2.2 A	UVLO with reference to GND2	3 kV_{RMS}
UCC5320S	2.4 A	2.2 A	Split output	3 kV_{RMS}
UCC5350M	5 A	5 A	Miller clamp	3 kV_{RMS}
UCC5390E	10 A	10 A	UVLO with reference to GND2	3 kV_{RMS}
UCC5390S	10 A	10 A	Split output	3 kV_{RMS}

(1) The S, E, and M suffixes are part of the orderable part number. See the *机械、封装和可订购信息* section for the full orderable part number.
(2) For detailed isolation ratings, see the *Insulation Specifications* table.

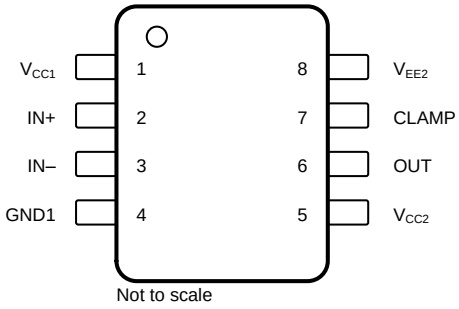
6 Pin Configuration and Function

UCC5320S and UCC5390S D Package
8-Pin SOIC
Top View



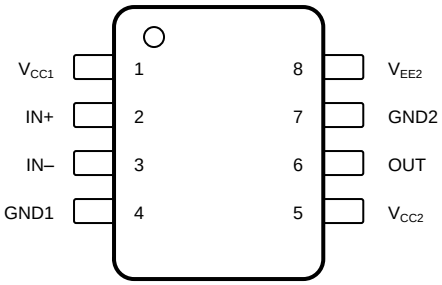
Not to scale

UCC5310M and UCC5350M D Package
8-Pin SOIC
Top View



Not to scale

UCC5320E and UCC5390E D Package
8-Pin SOIC
Top View



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Pin Functions

PIN				TYPE(1)	DESCRIPTION
NAME	NO.				
	UCC53x0S	UCC53x0M	UCC53x0E		
CLAMP	—	7	—	I	Active Miller-clamp input found on the UCC5310M and UCC5350M used to prevent false turnon of the power switches.
GND1	4	4	4	G	Input ground. All signals on the input side are referenced to this ground.
GND2	—	—	7	G	Gate-drive common pin. Connect this pin to the IGBT emitter. UVLO referenced to GND2 in the UCC5320E and UCC5390E variations.
IN+	2	2	2	I	Noninverting gate-drive voltage-control input. The IN+ pin has a CMOS input threshold. This pin is pulled low internally if left open. Use 表 4 to understand the input and output logic of these devices.
IN–	3	3	3	I	Inverting gate-drive voltage control input. The IN– pin has a CMOS input threshold. This pin is pulled high internally if left open. Use 表 4 to understand the input and output logic of these devices.
OUT	—	6	6	O	Gate-drive output for E and M versions.
OUTH	6	—	—	O	Gate-drive pullup output found on the UCC5320S and UCC5390S.
OUTL	7	—	—	O	Gate-drive pulldown output found on the UCC5320S and UCC5390S.
V_{CC1}	1	1	1	P	Input supply voltage. Connect a locally decoupled capacitor to GND. Use a low-ESR or ESL capacitor located as close to the device as possible.
V_{CC2}	5	5	5	P	Positive output supply rail. Connect a locally decoupled capacitor to V_{EE2}. Use a low-ESR or ESL capacitor located as close to the device as possible.
V_{EE2}	8	8	8	P	Negative output supply rail for E version, and GND for S and M versions. Connect a locally decoupled capacitor to GND2 for E version. Use a low-ESR or ESL capacitor located as close to the device as possible.

(1) P = Power, G = Ground, I = Input, O = Output

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input bias pin supply voltage	V_{CC1} – GND1	GND1 – 0.3	18	V
Driver bias supply	V_{CC2} – V_{EE2}	–0.3	35	V
V_{EE2} bipolar supply voltage for E version	V_{EE2} – GND2	–17.5	0.3	V
Output signal voltage	V_{OUTH} – V_{EE2}, V_{OUTL} – V_{EE2}, V_{OUT} – V_{EE2}, V_{CLAMP} – V_{EE2}	V_{EE2} – 0.3	V_{CC2} + 0.3	V
Input signal voltage	V_{IN+} – GND1, $V_{IN–}$ – GND1	GND1 – 5	V_{CC1} + 0.3	V
Junction temperature, T_J(2)		–40	150	°C
Storage temperature, T_{stg}			150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) To maintain the recommended operating conditions for T_J, see the *Thermal Information*.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS–001(1)	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CC1}	Supply voltage, input side	3		15	V
V_{CC2}	Positive supply voltage output side (V_{CC2} – V_{EE2})	13.2		33	V
V_{EE2}	Bipolar supply voltage for E version (V_{EE2} – GND2)	–16		0	V
V_{SUP2}	Total supply voltage output side (V_{CC2} – V_{EE2})	13.2		33	V
T_A	Ambient temperature	–40		125	°C

7.4 Thermal Information

THERMAL METRIC(1)		UCC53x0 D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction–to-ambient thermal resistance	109.5	°C/W
$R_{\theta JC(top)}$	Junction–to-case (top) thermal resistance	43.1	°C/W
$R_{\theta JB}$	Junction–to-board thermal resistance	51.2	°C/W
Ψ_{JT}	Junction–to-top characterization parameter	18.3	°C/W
Ψ_{JB}	Junction–to-board characterization parameter	50.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation on input and output	V_{CC1} = 5 V, V_{CC2} = 15 V, IN+ = 3.3 V, IN– = GND1, 687-kHz, 50% duty cycle, square wave, 2.4-nF load			1.14	W
P_{D1}	Maximum input power dissipation	V_{CC1} = 5 V, V_{CC2} = 15 V, IN+ = 3.3 V, IN– = GND1, 687-kHz, 50% duty cycle, square wave, 2.4-nF load			0.05	W
P_{D2}	Maximum output power dissipation	V_{CC1} = 5 V, V_{CC2} = 15 V, IN+ = 3.3 V, IN– = GND1, 687-kHz, 50% duty cycle, square wave, 2.4-nF load			1.09	W

7.6 Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE	UNIT
CLR	External Clearance(1)	Shortest pin–to-pin distance through air	4	mm
CPG	External Creepage(1)	Shortest pin–to-pin distance across the package surface	4	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	> 21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303–11); IEC 60112	> 600	V
	Material Group	According to IEC 60664–1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	
DIN V VDE 0884–10 (VDE V 0884–10): 2016–2012(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	990	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave); time dependent dielectric breakdown (TDDB) test	700	V_{RMS}
			990	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$ t = 60 s (qualification) t = 1 s (100% production)	4242	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(3)	Test method per IEC 60065, 1.2/50 µs waveform, $V_{TEST} = 1.3 \times V_{IOSM}$ (qualification)	4242	V_{PK}
q_{pd}	Apparent charge(4)	Method a: After I/O safety test subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a: After environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output(5)	$V_{IO} = 0.4 \times \sin(2\pi ft)$, f = 1 MHz	1.2	pF
R_{IO}	Isolation resistance, input to output(5)	V_{IO} = 500 V, T_A = 25°C	$> 10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$> 10^{11}$	
		V_{IO} = 500 V, T_S = 150°C	$> 10^{9}$	
	Pollution degree		2	
	Climatic category		40/125/21	
UL 1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$= 3000 V_{RMS}, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$ = 3600 V_{RMS} , t = 1 s (100% production)	3000	V_{RMS}

(1) Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a printed circuit board are used to help increase these specifications.
(2) This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

7.7 Safety-Related Certifications

VDE	CSA	UL	CQC
Certified according to DIN V VDE V 0884–10 (VDE V 0884–10):2006–12 and DIN EN 61010-1 (VDE 0411-1):2011-07	Plan to certify according CSA Component Acceptance Notice 5A, IEC 60950–1 and IEC 61010-1	Plan to certify according to UL 1577 Component Recognition Program	Plan to certify according to GB 4943.1–2011
Basic Insulation Maximum Transient isolation Overvoltage, 4242 V_{PK}; Maximum Repetitive Peak Voltage, 990 V_{PK}; Maximum Surge Isolation Voltage, 4242 V_{PK}	Basic insulation and Reinforced insulation per CSA 60950-1-07+A1+A2 and IEC 60950-1 2nd Ed.+A1+A2; Basic insulation working voltage per CSA 61010-1-12 and IEC 61010-1 3rd Ed.	Single protection, 3000 V_{RMS}	Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250V $_{RMS}$ maximum working voltage
Certification planned	Certification planned	Certification planned	Certification planned

7.8 Safety Limiting Values

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
D PACKAGE							
I_S	Safety output supply current	$R_{\theta JA}$ = 109.5°C/W, V_{CC2} = 15 V, T_J = 150°C, T_A = 25°C, see 图 1	Output side			76	mA
		$R_{\theta JA}$ = 109.5°C/W, V_{CC2} = 30 V, T_J = 150°C, T_A = 25°C, see 图 1	Output side			38	
P_S	Safety output supply power	$R_{\theta JA}$ = 109.5°C/W, T_J = 150°C, T_A = 25°C, see 图 2	Input side			0.05	W
			Output side			1.09	
			Total			1.14	
T_S	Maximum safety temperature					150	°C

(1) The safety-limiting constraint is the maximum junction temperature specified in the data sheet. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

7.9 Electrical Characteristics

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, T_A = –40°C to +125°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENTS						
I_{VCC1}	Input supply quiescent current	IN+ and IN- left floating		1.67	2.4	mA
I_{VCC2}	Output supply quiescent current	IN+ and IN- left floating		1.1	1.8	mA
SUPPLY VOLTAGE UNDERVOLTAGE THRESHOLDS						
$V_{IT+(UVLO1)}$	VCC1 Positive-going UVLO threshold voltage			2.6	2.8	V
$V_{IT-(UVLO1)}$	VCC1 Negative-going UVLO threshold voltage		2.4	2.5		V
$V_{hys(UVLO1)}$	VCC1 UVLO threshold hysteresis			0.1		V
$V_{IT+(UVLO2)}$	VCC2 Positive-going UVLO threshold voltage			12	13	V
$V_{IT-(UVLO2)}$	VCC2 Negative-going UVLO threshold voltage		10.3	11		V
$V_{hys(UVLO2)}$	VCC2 UVLO threshold voltage hysteresis			1		V
LOGIC I/O						
$V_{IT+(IN)}$	Positive-going input threshold voltage (IN+, IN–)			0.55 × V_{CC1}	0.7 × V_{CC1}	V
$V_{IT-(IN)}$	Negative-going input threshold voltage (IN+, IN–)		0.3 × V_{CC1}	0.45 × V_{CC1}		V
$V_{hys(IN)}$	Input hysteresis voltage (IN+, IN–)			0.1 × V_{CC1}		V
I_{IH}	High-level input leakage at IN+	IN+ = V_{CC1}		40	240	µA
I_{IL}	Low-level input leakage at IN–	IN– = GND1	–240	–40		µA
		IN– = GND1 – 5 V	–310	–80		
GATE DRIVER STAGE						
V_{OH}	High-level output voltage (OUT and OUTH)	I_{OUT} = –20 mA	V_{CC2} – 0.1	V_{CC2} – 0.24		V
V_{OL}	Low level output voltage (OUT and OUTL)	UCC5320S and UCC5320E, IN+ = low, IN– = high; I_O = 20 mA	9.4	13		mV
		UCC5310M, IN+ = low, IN– = high; I_O = 20 mA	17	26		
		UCC5390S and UCC5390E, IN+ = low, IN– = high; I_O = 20 mA	2	3		
		UCC5350M, IN+ = low, IN– = high; I_O = 20 mA	5	7		
I_{OH}	Peak source current	UCC5320S and UCC5320E, IN+ = high, IN– = low	2.4	4.3		A
		UCC5310M, IN+ = high, IN– = low	2.4	4.3		
		UCC5390S and UCC5390E, IN+ = high, IN– = low	10	17		
		UCC5350M, IN+ = high, IN– = low	5	10		

Electrical Characteristics (continued)

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, T_A = –40°C to +125°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OL}	Peak sink current	UCC5320S and UCC5320E, IN+ = low, IN– = high	2.2	4.4		A
		UCC5310M, IN+ = low, IN– = high	1.1	2.2		
		UCC5390S and UCC5390E, IN+ = low, IN– = high	10	17		
		UCC5350M, IN+ = low, IN– = high	5	10		
ACTIVE MILLER CLAMP (UCC53xxM only)						
V_{CLAMP}	Low-level clamp voltage	UCC5310M, I_{CLAMP} = 20 mA		26	50	mV
		UCC5350M, I_{CLAMP} = 20 mA		7	10	
I_{CLAMP}	Clamp low-level current	UCC5310M, V_{CLAMP} = V_{EE2} + 15 V	1.1	2.2		A
		UCC5350M, V_{CLAMP} = V_{EE2} + 15 V	5	10		
$I_{CLAMP(L)}$	Clamp low-level current for low output voltage	UCC5310M, V_{CLAMP} = V_{EE2} + 2 V	0.7	1.5		A
		UCC5350M, V_{CLAMP} = V_{EE2} + 2 V	5	10		
$V_{CLAMP-TH}$	Clamp threshold voltage	UCC3510M and UCC5350M		2.1	2.3	V
SHORT CIRCUIT CLAMPING						
$V_{CLP-OUT}$	Clamping voltage (V_{OUTH} – V_{CC2} or V_{OUT} –V_{CC2})	IN+ = high, IN– = low, t_{CLAMP} = 10 µs, I_{OUTH} or I_{OUT}= 500 mA		1	1.3	V
$V_{CLP-OUT}$	Clamping voltage (V_{EE2} – V_{OUTL} or V_{EE2} – V_{CLAMP} or V_{EE2} – V_{OUT})	IN+ = low, IN– = high, t_{CLAMP} = 10 µs, I_{CLAMP} or I_{OUTL} = –500 mA		1.5		V
		IN+ = low, IN– = high, I_{CLAMP} or I_{OUTL} = –20 mA		0.9	1	
ACTIVE PULLDOWN						
V_{OUTSD}	Active pulldown voltage on OUTL, CLAMP, OUT	UCC5320S, UCC5320E, and UCC5310M I_{OUTL} or I_{OUT} = 0.1 × $I_{OUTL(typ)}$, V_{CC2} = open		1.8	2.5	V

7.10 Switching Characteristics

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, T_A = –40°C to +125°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output-signal rise time	UCC5320S, UCC5320E, and UCC5310M, C_{LOAD} = 1 nF		12	28	ns
		UCC5390S, UCC5390E, and UCC5350M, C_{LOAD} = 1 nF		10	26	ns
t_f	Output-signal fall time	UCC5320S and UCC5320E, C_{LOAD} = 1 nF		10	25	ns
		UCC5310M, C_{LOAD} = 1 nF		10	26	ns
		UCC5390S, UCC5390E, and UCC5350M, C_{LOAD} = 1 nF		10	22	ns
t_{PLH}	Propagation delay (default versions), high	UCC5320S and UCC5320E, C_{LOAD} = 100 pF		60	72	ns
		UCC5310M, C_{LOAD} = 100 pF		60	75	ns
		UCC5390S, UCC5390E, and UCC5350M, C_{LOAD} = 100 pF		65	100	ns
t_{PHL}	Propagation delay (default versions), low	UCC5320S and UCC5320E, C_{LOAD} = 100 pF		60	75	ns
		UCC5310M, C_{LOAD} = 100 pF		60	75	ns
		UCC5390S, UCC5390E, and UCC5350M, C_{LOAD} = 100 pF		65	100	ns
t_{UVLO1_rec}	UVLO recovery delay of V_{CC1}			30		µs
t_{UVLO2_rec}	UVLO recovery delay of V_{CC2}			50		µs

Switching Characteristics (continued)

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, T_A = –40°C to +125°C, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PWD}	Pulse width distortion $\lvert t_{PHL} - t_{PLH} \rvert$	UCC5320S and UCC5320E, C_{LOAD} = 100 pF		1	20	ns
		UCC5310M, C_{LOAD} = 100 pF		1	20	ns
		UCC5390S and UCC5390E, C_{LOAD} = 100 pF		1	20	ns
		UCC5350M, C_{LOAD} = 100 pF		1	20	ns
$t_{sk(pp)}$	Part-to-part skew(1)	UCC5320S and UCC5320E, C_{LOAD} = 100 pF		1	25	ns
		UCC5310M, C_{LOAD} = 100 pF		1	25	ns
		UCC5390S and UCC5390E, C_{LOAD} = 100 pF		1	25	ns
		UCC5350M, C_{LOAD} = 100 pF		1	25	ns
CMTI	Common-mode transient immunity	PWM is tied to GND or V_{CC1}, V_{CM} = 1200 V	100	120		kV/µs

(1) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between the output of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads guaranteed by characterization.

7.11 Insulation Characteristics Curves

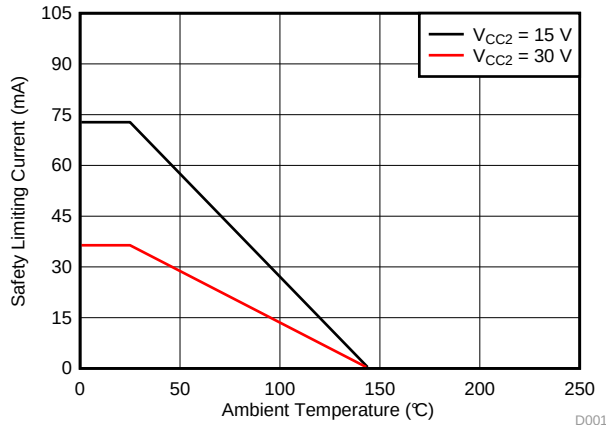


图 1. Thermal Derating Curve for Limiting Current per VDE

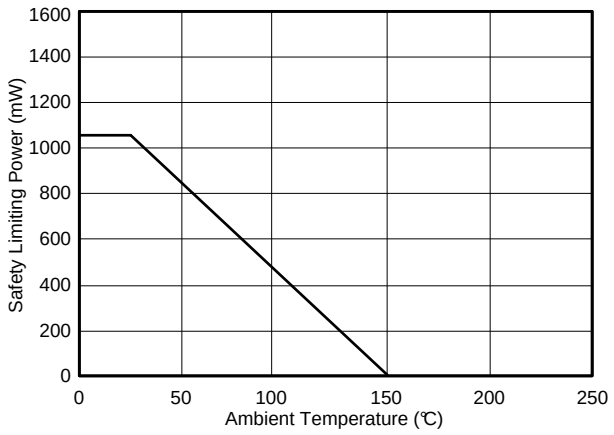
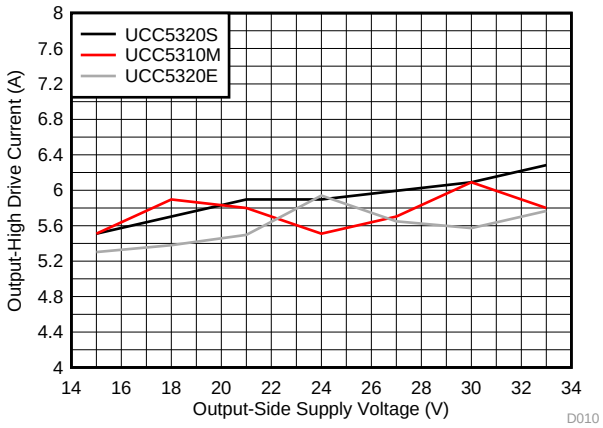


图 2. Thermal Derating Curve for Limiting Power per VDE

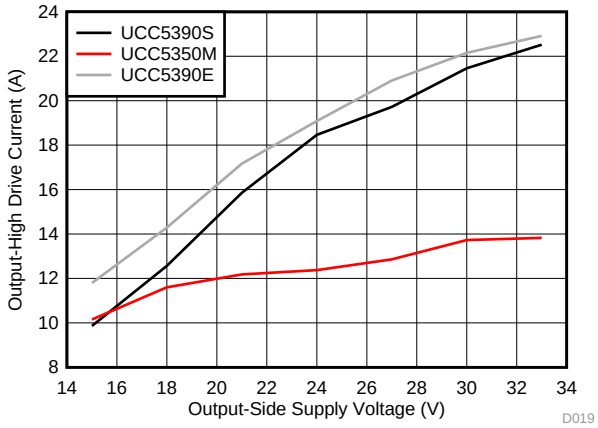
7.12 Typical Characteristics

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_A = –40°C to +125°C, (unless otherwise noted)



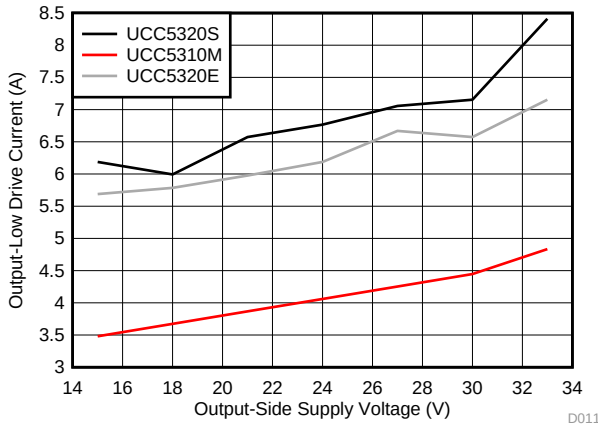
C_{LOAD} = 150 nF

图 3. Output-High Drive Current vs Output Voltage



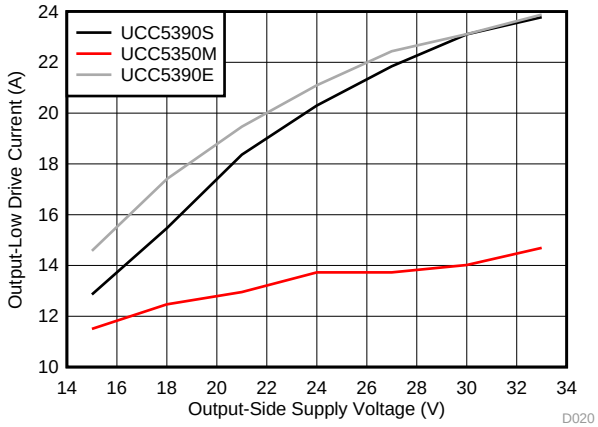
C_{LOAD} = 150 nF

图 4. Output-High Drive Current vs Output Voltage



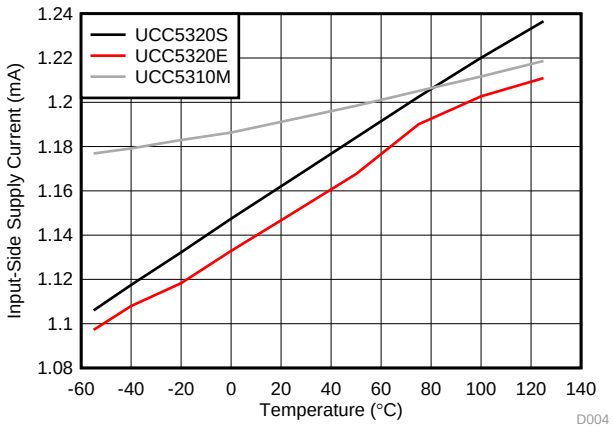
C_{LOAD} = 150 nF

图 5. Output-Low Drive Current vs Output Voltage



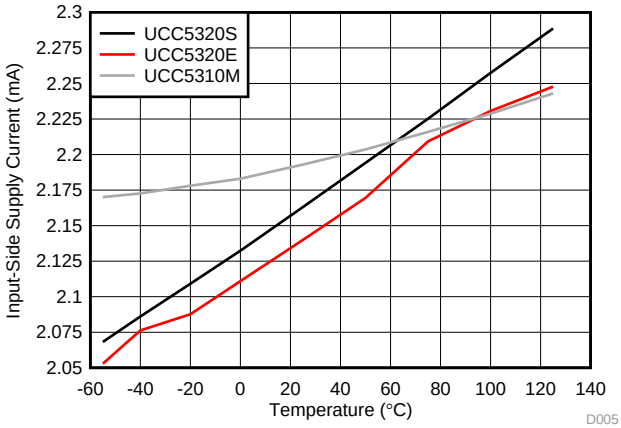
C_{LOAD} = 150 nF

图 6. Output-Low Drive Current vs Output Voltage



IN+ = L IN– = H

图 7. I_{CC1} Supply Current vs Temperature

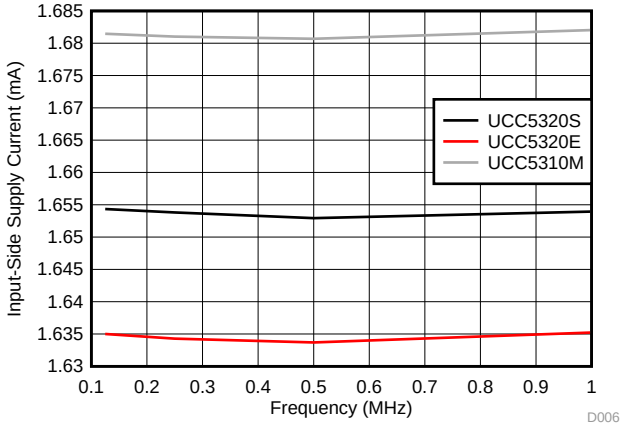


IN+ = H IN– = L

图 8. I_{CC1} Supply Current vs Temperature

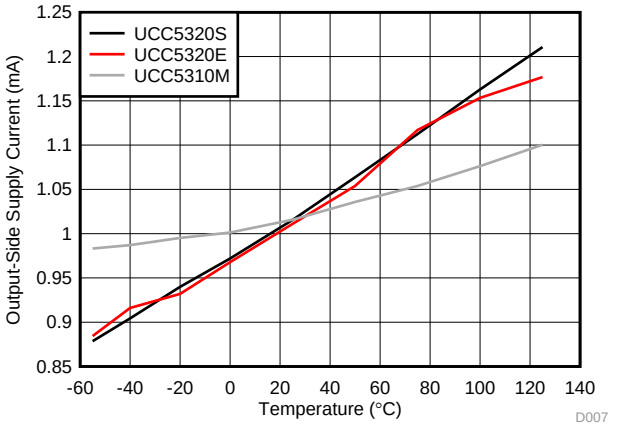
Typical Characteristics (接下页)

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_A = –40°C to +125°C, (unless otherwise noted)



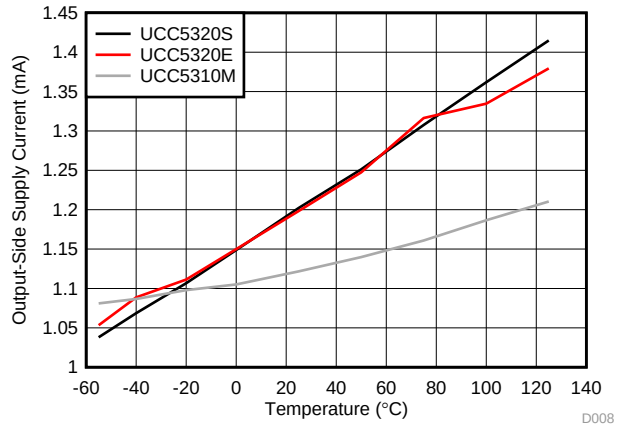
Duty Cycle = 50% T = 25°C

图 9. I_{CC1} Supply Current vs Input Frequency



Duty Cycle = 50% IN+ = L IN– = H

图 10. I_{CC2} Supply Current vs Temperature



Duty Cycle = 50% IN+ = H IN– = L

图 11. I_{CC2} Supply Current vs Input Frequency

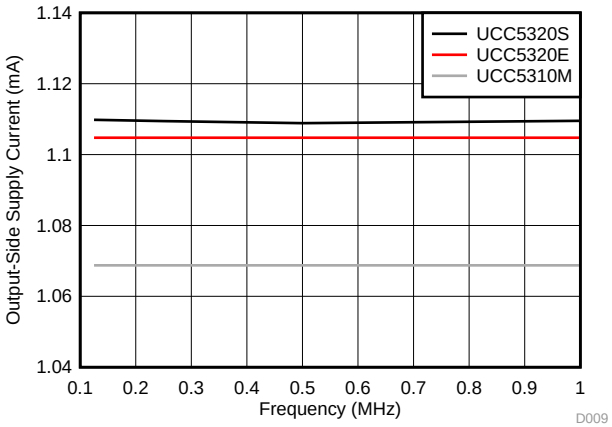
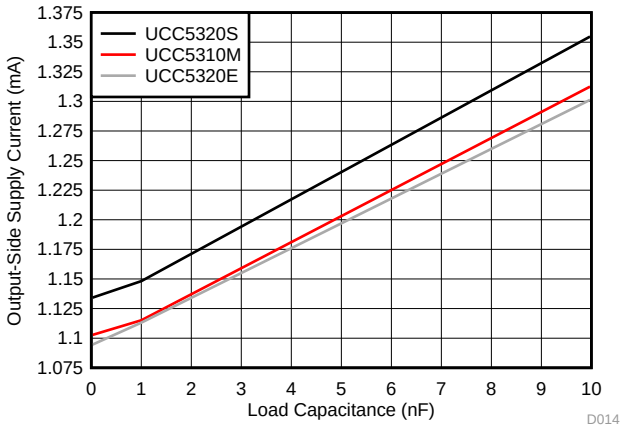
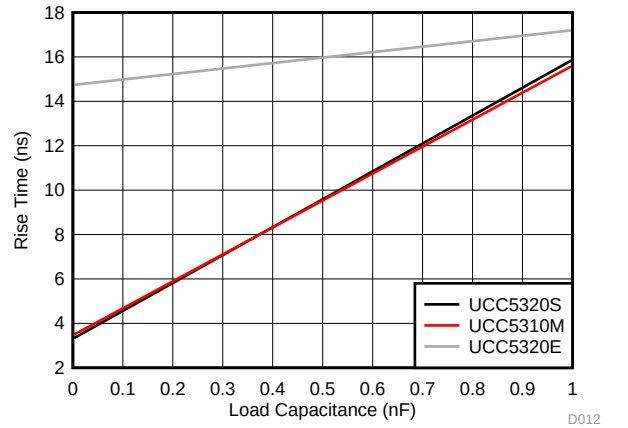


图 12. I_{CC2} Supply Current vs Input Frequency



f_{SW} = 1 kHz

图 13. I_{CC2} Supply Current vs Load Capacitance

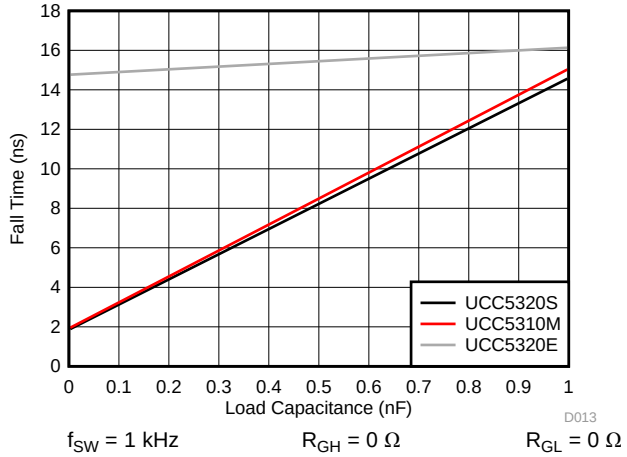


f_{SW} = 1 kHz R_{GH} = 0 Ω R_{GL} = 0 Ω

图 14. Rise Time vs Load Capacitance

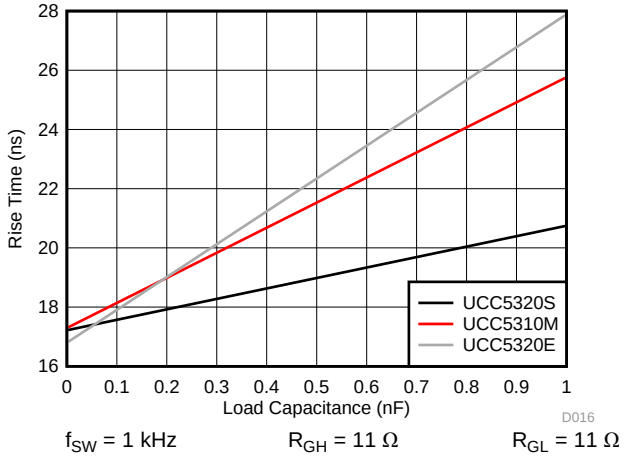
Typical Characteristics (接下页)

V_{CC1} = 3.3 V or 5 V, 0.1-µF capacitor from V_{CC1} to GND1, V_{CC2}= 15 V, 1-µF capacitor from V_{CC2} to V_{EE2}, C_{LOAD} = 1 nF, T_A = –40°C to +125°C, (unless otherwise noted)



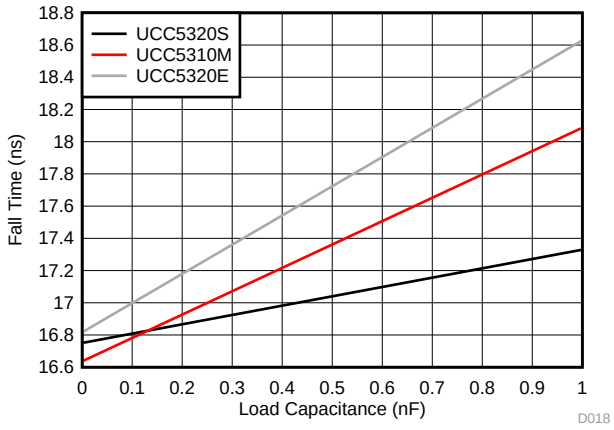
f_{SW} = 1 kHz R_{GH} = 0 Ω R_{GL} = 0 Ω

图 15. Fall Time vs Load Capacitance



f_{SW} = 1 kHz R_{GH} = 11 Ω R_{GL} = 11 Ω

图 16. Rise Time vs Load Capacitance



f_{SW} = 1-kHz R_{GH} = 11 Ω R_{GL} = 11 Ω

图 17. Fall Time vs Load Capacitance

8 Parameter Measurement Information

8.1 Propagation Delay, Inverting, and Noninverting Configuration

图 18 shows the propagation delay OUTH and OUTL for noninverting configurations. 图 19 shows the propagation delay with the inverting configuration. These figures also demonstrate the method used to measure the rise (t_r) and fall (t_f) times.

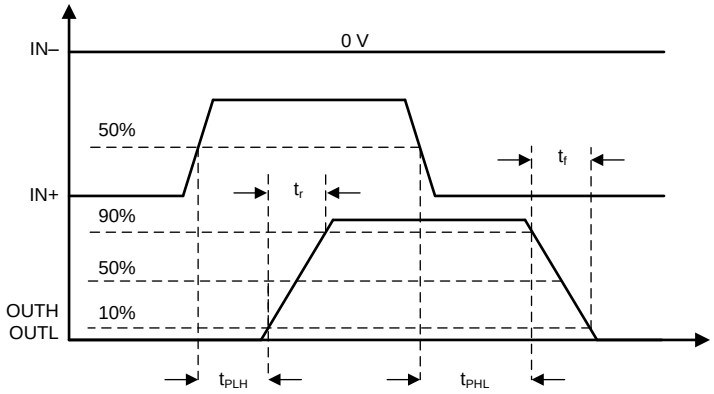


图 18. OUTH and OUTL Propagation Delay, Noninverting Configuration

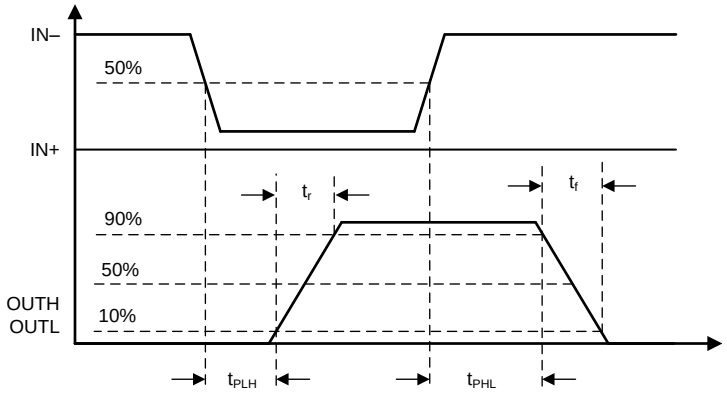


图 19. OUTH and OUTL Propagation Delay, Inverting Configuration

Propagation Delay, Inverting, and Noninverting Configuration (接下页)

8.1.1 CMTI Testing

图 20, 图 21, and 图 22 are simplified diagrams of the CMTI testing configuration used for each device type.

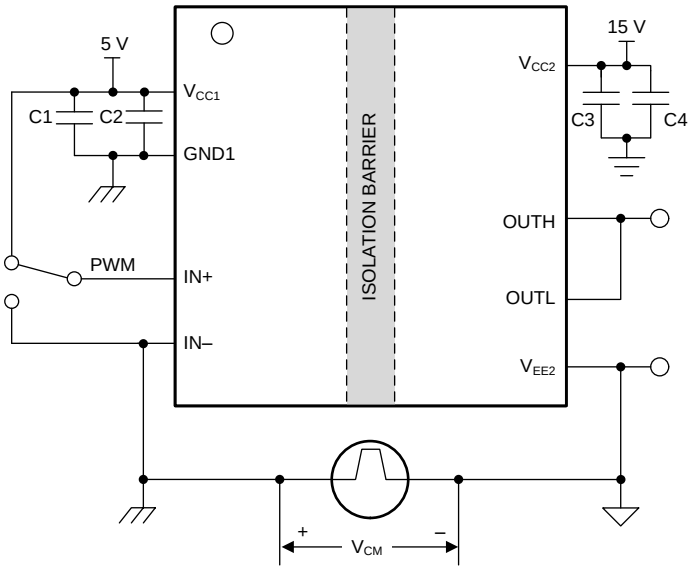


图 20. CMTI Test Circuit for UCC5320S and UCC5390S

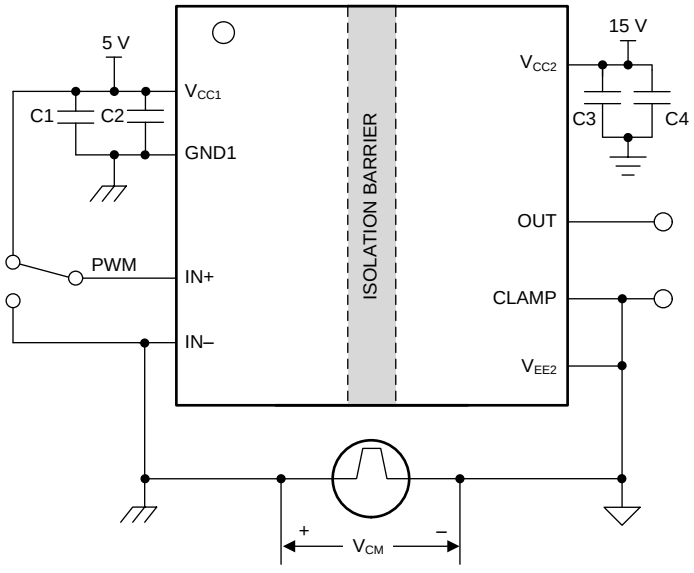


图 21. CMTI Test Circuit for UCC5310M and UCC5350M

Propagation Delay, Inverting, and Noninverting Configuration (接下页)

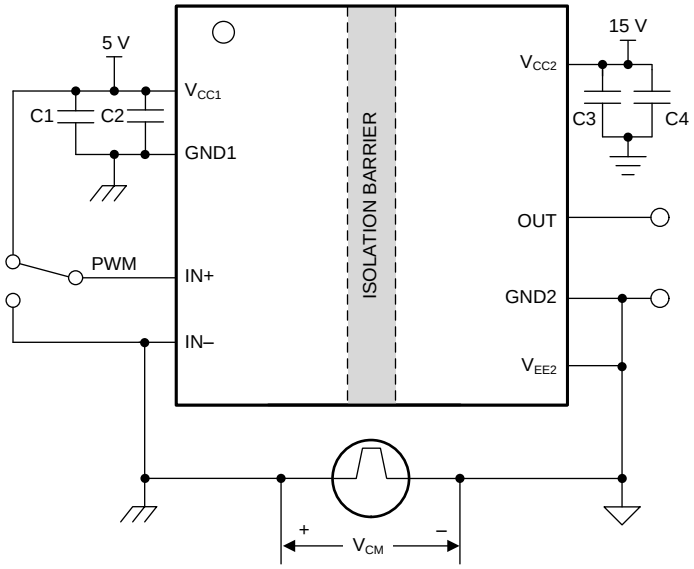


图 22. CMTI Test Circuit for UCC5320E and UCC5390E

9 Detailed Description

9.1 Overview

The UCC53x0 family of isolated gate drivers with variations for built-in split output, Miller clamp, and UVLO2 referenced to GND2 (see Device Comparison Table). The isolation inside the UCC53x0 family of devices is implemented with high-voltage SiO_2-based capacitors. The signal across the isolation has an on-off keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier (see 图 24). The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. The UCC53x0 devices also incorporate advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions from the high frequency carrier and IO buffer switching. The conceptual block diagram of a digital capacitive isolator, 图 23, shows a functional block diagram of a typical channel. 图 24 shows a conceptual detail of how the OOK scheme works.

图 23 shows how the input signal passes through the capacitive isolation barrier through modulation (OOK) and signal conditioning. 图 24 shows the OOK-based modulation scheme.

9.2 Functional Block Diagram

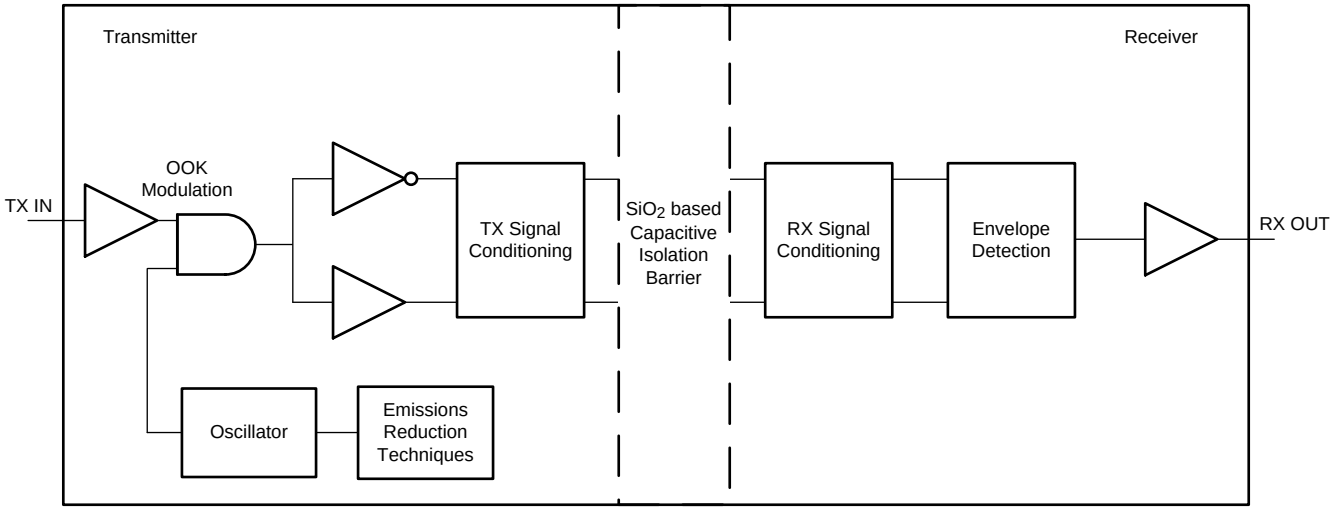


图 23. Conceptual Block Diagram of a Capacitive Data Channel

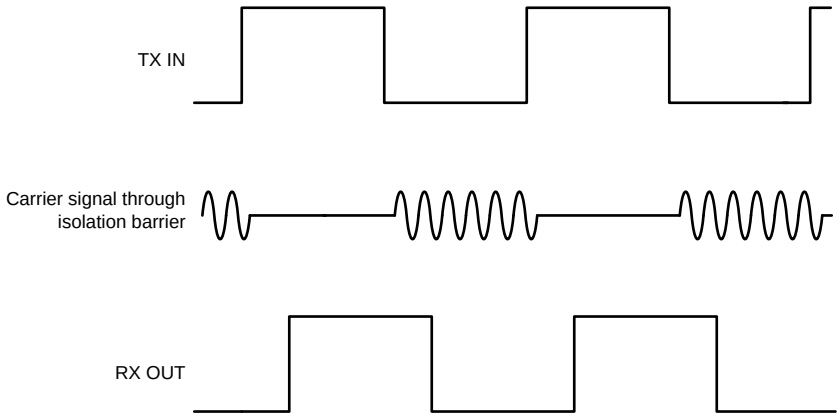


图 24. On-Off Keying (OOK) Based Modulation Scheme

Functional Block Diagram (接下页)

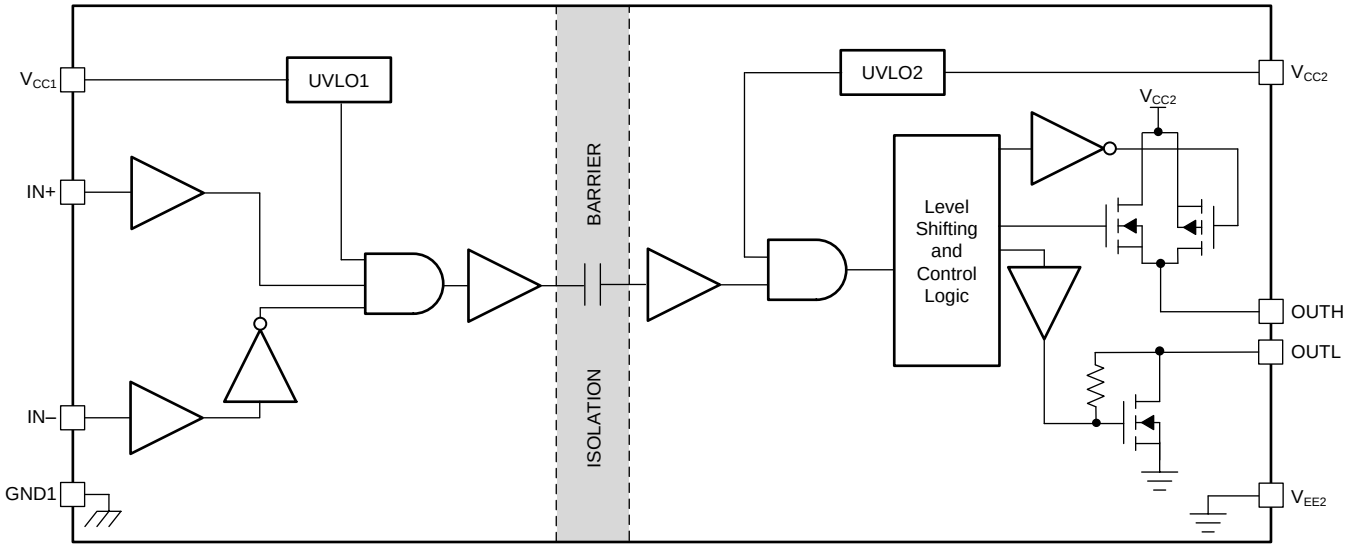


图 25. Functional Block Diagram—UCC5320S and UCC5390S Split Outputs

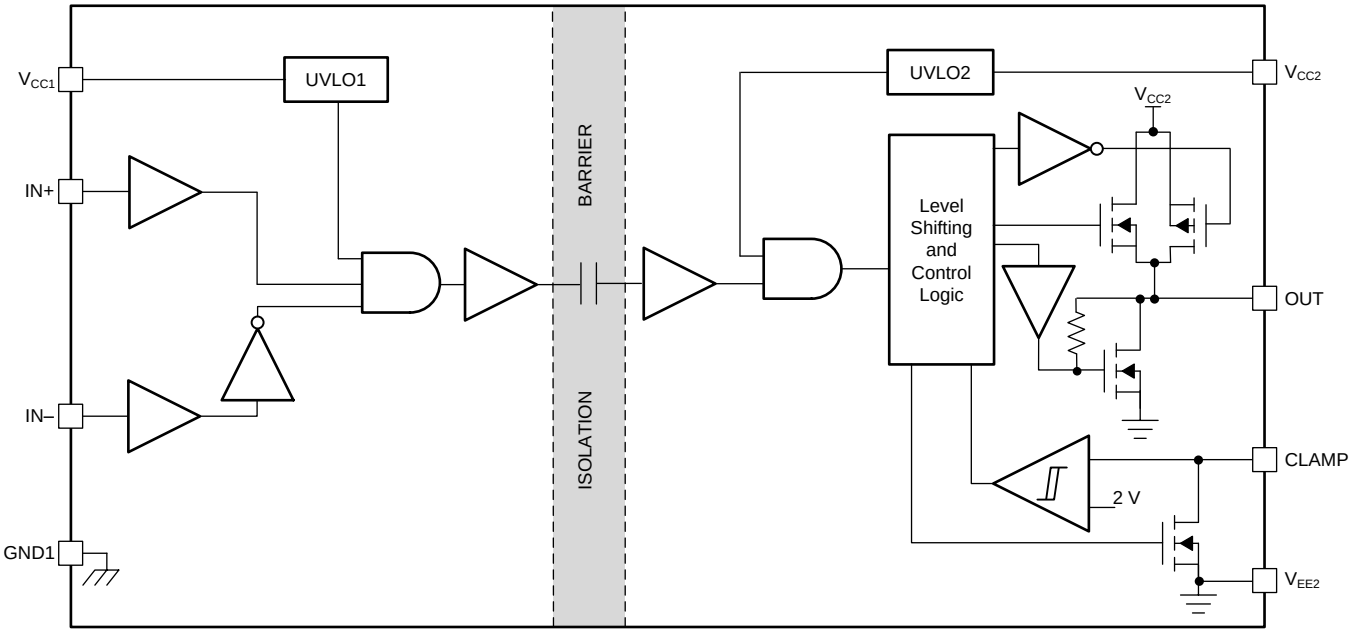


图 26. Functional Block Diagram—UCC5310M and UCC5350 Miller Clamp

Functional Block Diagram (接下页)

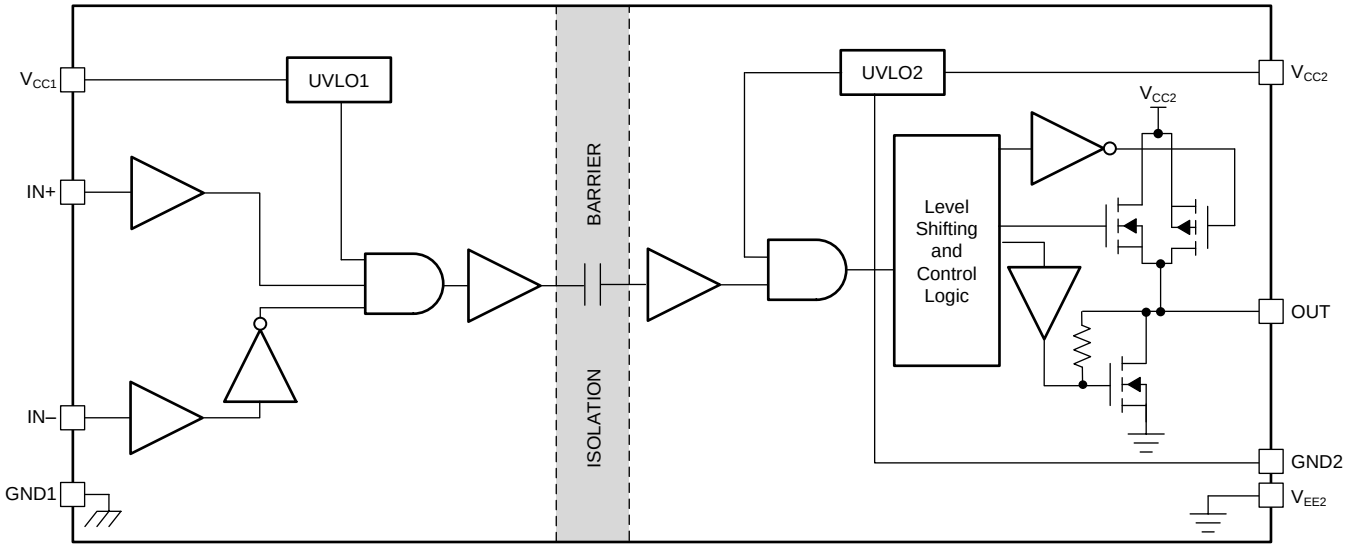


图 27. Functional Block Diagram—UCC5320E and UCC5390E UVLO With Respect to GND2

9.3 Feature Description

9.3.1 Power Supply

The V_{CC1} input power supply supports a wide voltage range from 3 V to 15 V and the V_{CC2} output supply supports a voltage range from 13.2 V to 33 V. For operation with bipolar supplies, the power device is turned off with a negative voltage on the gate with respect to the emitter or source. This configuration prevents the power device from unintentionally turning on because of current induced from the Miller effect. The typical values of the V_{CC2} and V_{EE2} output supplies for bipolar operation are 15 V and –8 V with respect to GND2 for IGBTs, and 20 V and –5 V for SiC MOSFETs.

For operation with unipolar supply, the V_{CC2} supply is connected to 15 V with respect to GND2 for IGBTs, and 20 V for SiC MOSFETs. The V_{EE2} supply is connected to 0 V. In this use case, the UCC53x0 device with Miller clamping function (UCC53x0M) can be used. The Miller clamping function is implemented by adding a low impedance path between the gate of the power device and the V_{EE2} supply. Miller current can sink and the gate voltage is clamped to be lower than the turnon threshold value for the gate.

9.3.2 Input Stage

The input pins (IN+ and IN–) of UCC53x0 family are based on CMOS-compatible input-threshold logic that is completely isolated from the V_{CC2} supply voltage. The input pins are easy to drive with logic-level control signals (such as those from 3.3-V microcontrollers) because the UCC53x0 family has a typical high threshold ($V_{IT+(IN)}$) of 0.56 × V_{CC1} and a typical low threshold of 0.45 × V_{CC1}. A wide hysteresis ($V_{hys(IN)}$) of 0.1 × V_{CC1} makes for good noise immunity and stable operation. If any of the inputs are left open, 128 kΩ of internal pulldown resistance forces the IN+ pin low and 128 kΩ of internal resistance pulls IN– high. However, TI still recommends grounding an input if it is not being used for improved noise immunity.

Because the input side of the UCC53x0 family is isolated from the output driver, the input signal amplitude can be larger or smaller than V_{CC2} provided that it does not exceed the recommended limit. This feature allows greater flexibility when integrating the gate-driver with control signal sources, and allows the user to choose the most efficient V_{CC2} for any gate. However, the amplitude of any signal applied to IN+ or IN– must never be at a voltage higher than V_{CC1}.

Feature Description (接下页)

9.3.3 Output Stage

The output stages of the UCC53x0 family feature a pullup structure that delivers the highest peak-source current when it is most needed which is during the Miller plateau region of the power-switch turnon transition (when the power-switch drain or collector voltage experiences dV/dt). The output stage pullup structure features a P-channel MOSFET and an additional pullup N-channel MOSFET in parallel. The function of the N-channel MOSFET is to provide a brief boost in the peak-sourcing current, enabling fast turnon. Fast turnon is accomplished by briefly turning on the N-channel MOSFET during a narrow instant when the output is changing states from low to high. The on-resistance of this N-channel MOSFET (R_{NMOS}) is approximately 4.5 Ω when activated. 表 1 lists the typical internal-resistance values of the pullup and pulldown structure.

表 1. UCC53x0 On-Resistance

DEVICE OPTION	R_{NMOS}	R_{OH}	R_{OL}	R_{CLAMP}	UNIT
UCC5320S and UCC5320E	4.5	12	0.65	Not applicable	Ω
UCC5310M	4.5	12	1.3	1.3	Ω
UCC5390S and UCC5390E	0.76	12	0.13	Not applicable	Ω
UCC5350M	1.54	12	0.26	0.26	Ω

The R_{OH} parameter is a DC measurement and is representative of the on-resistance of the P-channel device only. This parameter is only for the P-channel device because the pullup N-channel device is held in the OFF state in DC condition and is turned on only for a brief instant when the output is changing states from low to high. Therefore, the effective resistance of the UCC53x0 pullup stage during this brief turnon phase is much lower than what is represented by the R_{OH} parameter, yielding a faster turnon. The turnon-phase output resistance is the parallel combination R_{OH} || R_{NMOS}.

The pulldown structure in the UCC53x0 S and E versions is simply composed of an N-channel MOSFET. For the M version, an additional FET is connected in parallel with the pulldown structure when the CLAMP and OUT pins are connected to the gate of the IGBT or MOSFET. The output of the UCC53x0 family is capable of delivering, or sinking, 2-A, 5-A and 10-A peak current pulses. The output voltage swing between V_{CC2} and V_{EE2} provides rail-to-rail operation because of the MOS-out stage which delivers very low dropout.

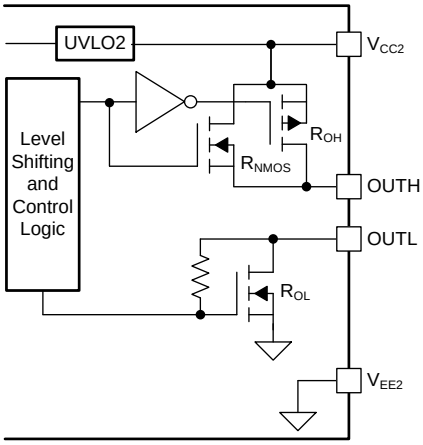


图 28. Output Stage—S Version

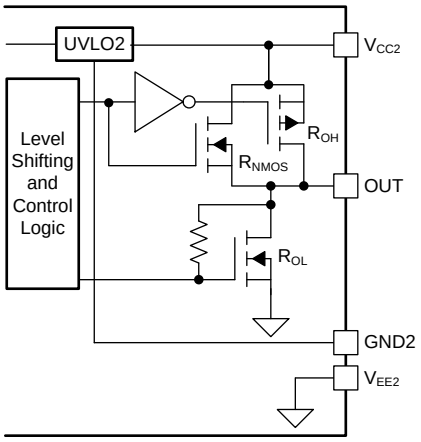


图 29. Output Stage—E Version

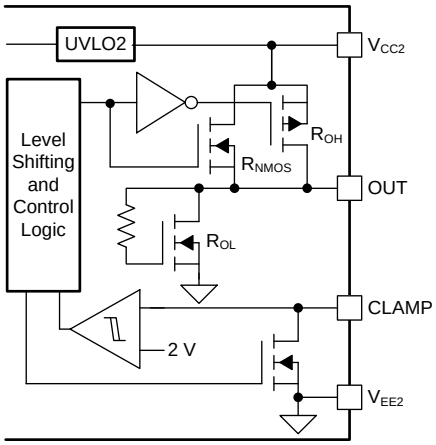


图 30. Output Stage—M Version

9.3.4 Protection Features

9.3.4.1 Undervoltage Lockout (UVLO)

UVLO functions are implemented for both the V_{CC1} and V_{CC2} supplies between the V_{CC1} and GND1, and V_{CC2} and V_{EE2} pins to prevent an underdriven condition on IGBTs and MOSFETs. When V_{CC} is lower than $V_{IT+\ (UVLO)}$ at device start-up or lower than $V_{IT-(UVLO)}$ after start-up, the voltage-supply UVLO feature holds the effected output low, regardless of the input pins (IN+ and IN–) as shown in 表 4. The V_{CC1} UVLO protection has a hysteresis feature ($V_{hys(UVLO1)}$). This hysteresis prevents chatter when the power supply produces ground noise which allows the device to permit small drops in bias voltage, which occurs when the device starts switching and operating current consumption increases suddenly. 图 31 shows the UVLO functions.

表 2. UCC53x0 V_{CC1} UVLO Logic

CONDITION	INPUTS		OUTPUTS	
	IN+	IN–	OUT, OUTH	OUTL
V_{CC1} – GND1 < $V_{IT+(UVLO1)}$ during device start-up	H	L	L	L
	L	H	L	L
	H	H	L	L
	L	L	L	L

表 2. UCC53x0 V_{CC1} UVLO Logic (接下页)

CONDITION	INPUTS		OUTPUTS	
	IN+	IN–	OUT, OUTH	OUTL
V_{CC1} – GND1 < $V_{IT–(UVLO1)}$ during device start-up	H	L	L	L
	L	H	L	L
	H	H	L	L
	L	L	L	L

表 3. UCC53x0 V_{CC2} UVLO Logic

CONDITION	INPUTS		OUTPUTS	
	IN+	IN–	OUT, OUTH	OUTL
V_{CC2} – V_{EE2} < $V_{IT+(UVLO2)}$ during device start-up	H	L	L	L
	L	H	L	L
	H	H	L	L
	L	L	L	L
V_{CC2} – V_{EE2} < $V_{IT–(UVLO2)}$ during device start-up	H	L	L	L
	L	H	L	L
	H	H	L	L
	L	L	L	L

When the output stages of the driver are in an unbiased or UVLO condition, the driver outputs are held low by an active clamp circuit that limits the voltage rise on the driver outputs. In this condition, the upper PMOS is resistively held off by a pullup resistor while the lower NMOS gate is tied to the driver output through a 500-kΩ resistor. In this configuration, the output is effectively clamped to the threshold voltage of the lower NMOS device which is typically less than 1.5 V when no bias power is available.

When V_{CC1} or V_{CC2} drops below the UVLO1 or UVLO2 threshold, a delay, t_{UVLO1_rec} or t_{UVLO2_rec}, occurs on the output when the supply voltage rises above $V_{IT+(UVLO)}$ or $V_{IT+(UVLO2)}$ again. 图 31 and 图 32 show this delay.

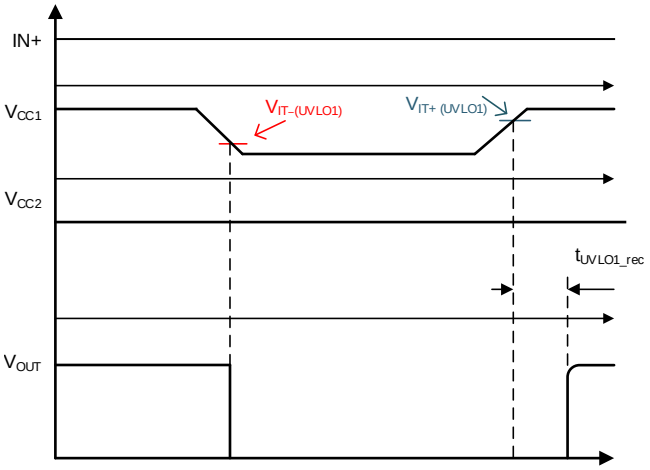


图 31. UVLO1 Functions

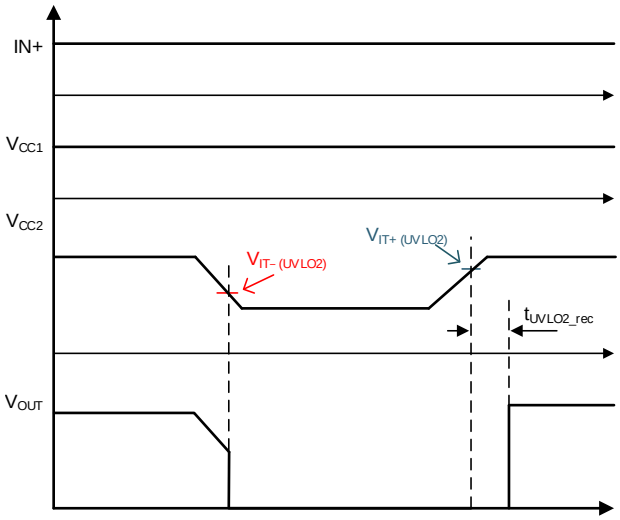


图 32. UVLO2 Functions

9.3.4.2 Active Pulldown

The active pulldown function is used to pull the IGBT or MOSFET gate to the low state when no power is connected to the V_{CC2} supply. This feature prevents false IGBT and MOSFET turnon on the OUT, OUTL, and CLAMP pins by clamping the output to approximately 2 V.

9.3.4.3 Short-Circuit Clamping

The short-circuit clamping function is used to clamp voltages at the driver output and pull the active Miller clamp pins slightly higher than the V_{CC2} voltage during short-circuit conditions. The short-circuit clamping function helps protect the IGBT or MOSFET gate from overvoltage breakdown or degradation. The short-circuit clamping function is implemented by adding a diode connection between the dedicated pins and the V_{CC2} pin inside the driver. The internal diodes can conduct up to 500-mA current for a duration of 10 µs and a continuous current of 20 mA. Use external Schottky diodes to improve current conduction capability as needed.

9.3.4.4 Active Miller Clamp (UCC53x0M)

The active Miller-clamp function is used to prevent false turnon of the power switches caused by Miller current in applications where a unipolar power supply is used. The active Miller-clamp function is implemented by adding a low impedance path between the power-switch gate terminal and ground (V_{EE2}) to sink the Miller current. With the Miller-clamp function, the power-switch gate voltage is clamped to less than 2 V during the off state. 图 36 shows a typical application circuit of UCC5310M and UCC5350M.

9.4 Device Functional Modes

表 4 lists the functional modes for the UCC53x0 devices.

表 4. Function Table(1)

V_{CC1}	V_{CC2}	IN+	IN–	OUTH, OUTL
PU	PD	X	X	Low
PD	PU	X	X	Low
PU	PU	Low	X	Low
PU	PU	X	High	Low
PU	PU	High	Low	High

(1) PU = Powered up (V_{CC1} ≥ 2.8 V or V_{CC2} ≥ 13 V); PD = Powered down (V_{CC1} ≤ 2.4 V or V_{CC2} ≤ 10.3 V); X = Irrelevant

9.4.1 Device I/O

图 33 shows the input and output structure of the UCC53x0 family of isolated gate drivers.

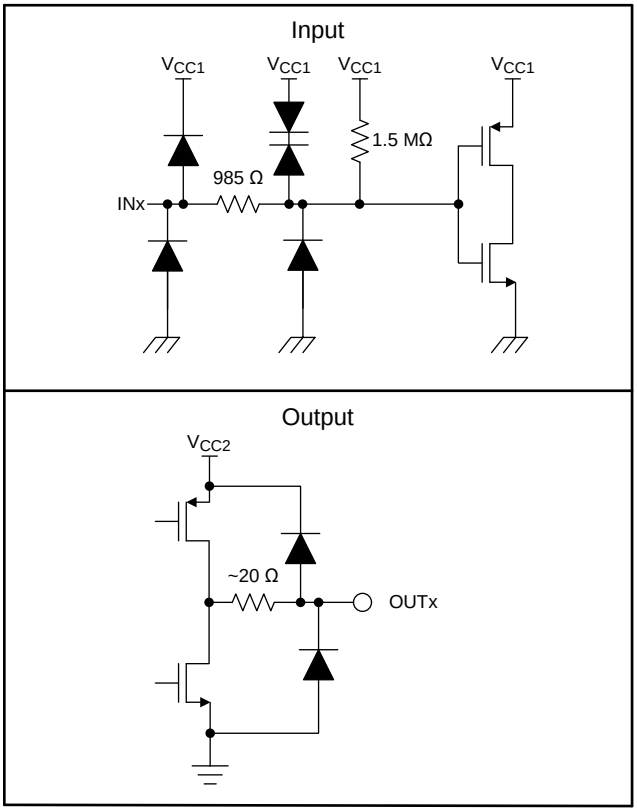


图 33. Device Input and Output Structure

9.4.2 ESD Structure

图 34 shows the multiple diodes involved in the ESD protection components of the UCC53x0 family. This provides pictorial representation of the absolute maximum rating for the device.

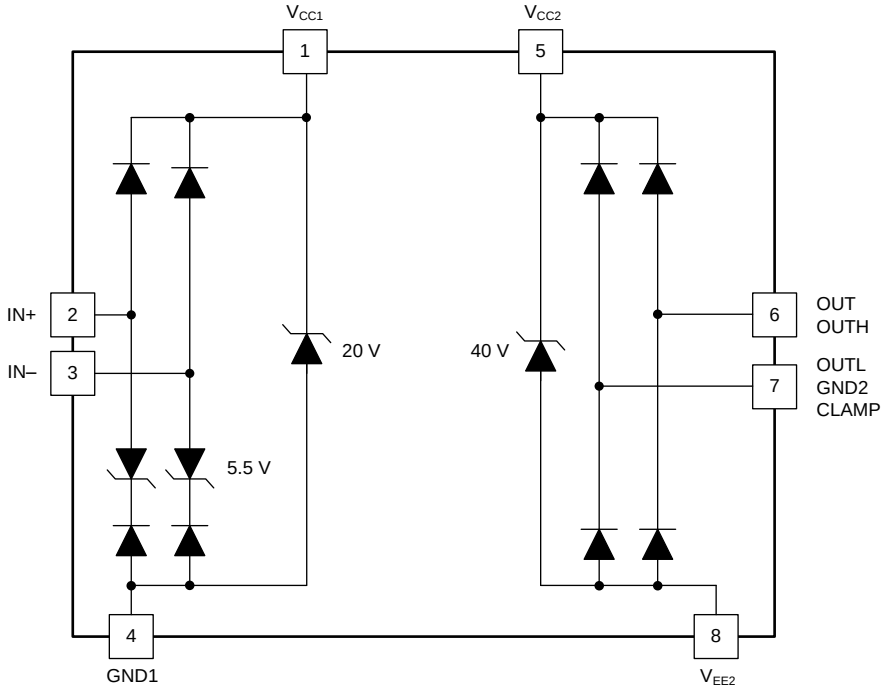


图 34. ESD Structure

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The UCC53x0 is a family of simple, isolated gate drivers for power semiconductor devices, such as MOSFETs, IGBTs, or SiC MOSFETs. The family of devices is intended for use in applications such as motor control, industrial inverters, and switched-mode power supplies.

The UCC53x0 family of devices has three pinout configurations, featuring split outputs, Miller clamp, and UVLO with reference to GND2. The UCC5320S and UCC5390S has two outputs, which are OUTH and OUTL. The two outputs can be used to separately decouple the power transistor turnon and turnoff commutations. The UCC5310M and UCC5350M feature active Miller clamping, which can be used to prevent false turnon of the power transistors induced by the Miller current. The UCC5320E and UCC5390E offer true UVLO protection by monitoring the voltage between the V_{CC2} and GND2 pins to prevent the power transistors from operating in a saturation region. The UCC53x0 family of devices comes in an 8-pin D package option and has a creepage, or clearance, of 4 mm, which is suitable for applications where basic isolation is required. Different drive strengths enable a simple driver platform to be used for applications demanding power transistors with different power ratings. Specifically, the UCC5390 device offers a 10-A drive current which can help remove the external current buffer used to drive high power transistors.

10.2 Typical Application

The circuits in 图 35, 图 36, and 图 37 show a typical application for driving IGBTs.

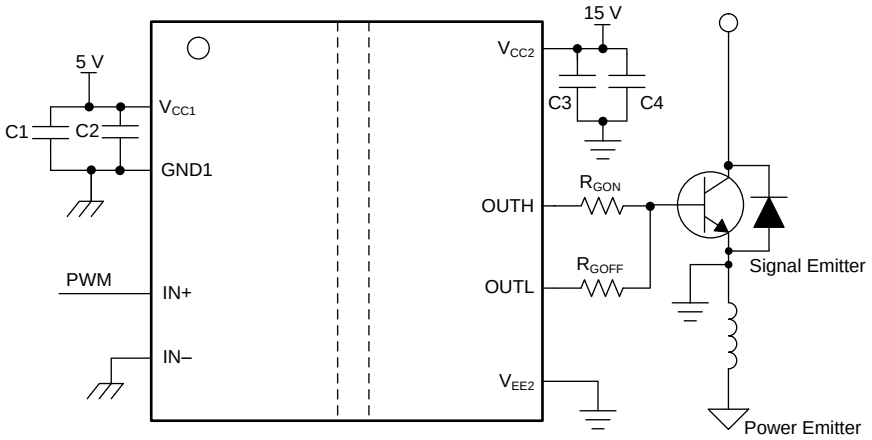


图 35. Typical Application Circuit for UCC5320S and UCC5390S to Drive IGBT

Typical Application (接下页)

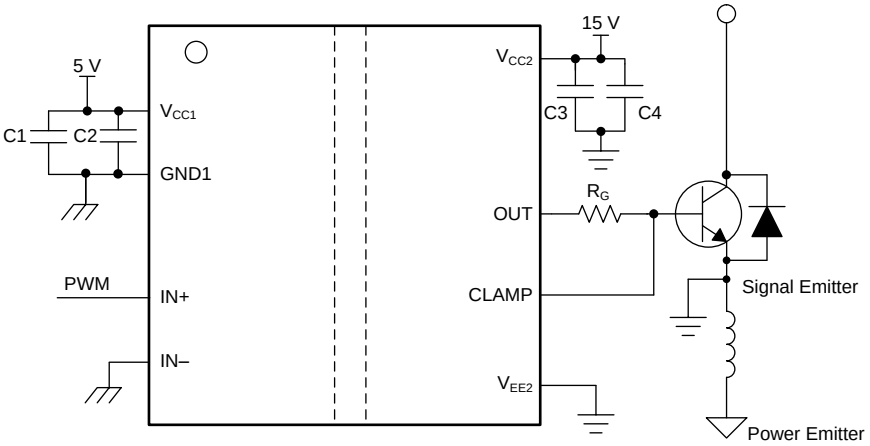


图 36. Typical Application Circuit for UCC5310M and UCC5350M to Drive IGBT

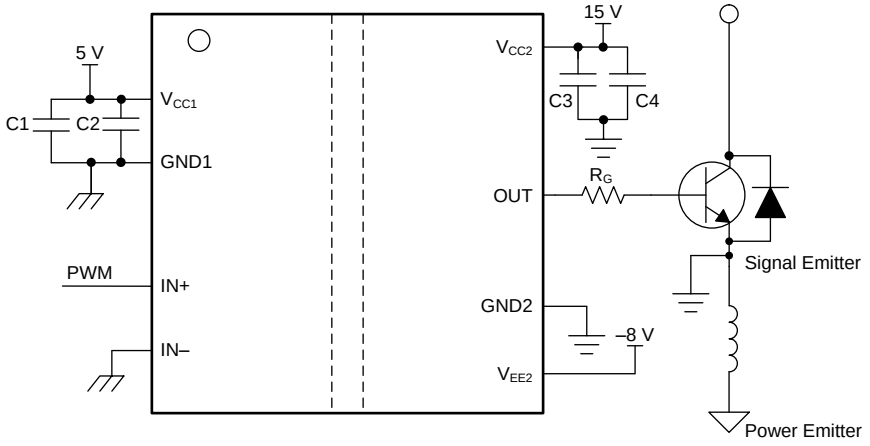


图 37. Typical Application Circuit for UCC5320E and UCC5390E to Drive IGBT

10.2.1 Design Requirements

表 5 lists the recommended conditions to observe the input and output of the UCC5320S split-output gate driver with the IN– pin tied to the GND1 pin.

表 5. UCC5320S Design Requirements

PARAMETER	VALUE	UNIT
V_{CC1}	5	V
V_{CC2}	20	V
IN+	5	V_{PP}
IN–	GND1	V
Switching frequency	1	kHz

10.2.2 Detailed Design Procedure

10.2.2.1 Designing IN+ and IN– Input Filter

TI recommends that users avoid shaping the signals to the gate driver in an attempt to slow down (or delay) the signal at the output. However, a small input filter, R_{IN}-C_{IN}, can be used to filter out the ringing introduced by nonideal layout or long PCB traces.

Such a filter should use an R_{IN} resistor with a value from 0 Ω to 100 Ω and a C_{IN} capacitor with a value from 10 pF to 100 pF. In the example, the selected value for R_{IN} is 51 Ω and C_{IN} is 33 pF, with a corner frequency of approximately 100 MHz.

When selecting these components, pay attention to the trade-off between good noise immunity and propagation delay.

10.2.2.2 Gate-Driver Output Resistor

The external gate-driver resistors, $R_{G(ON)}$ and $R_{G(OFF)}$ are used to:

1. Limit ringing caused by parasitic inductances and capacitances
2. Limit ringing caused by high voltage or high current switching dv/dt, di/dt, and body-diode reverse recovery
3. Fine-tune gate drive strength, specifically peak sink and source current to optimize the switching loss
4. Reduce electromagnetic interference (EMI)

The UCC53x0 devices have similar pullup structures but S and E variations have different pulldown circuits than the M version as described in the Output Stage section. The output stage has a pullup structure consisting of a P-channel MOSFET and an N-channel MOSFET in parallel. The combined peak source current is 4.3 A for the UCC5320 family and 17 A for the UCC5390 family. Use 公式 1 to estimate the peak source current using the UCC5320S as an example.

$$I_{OH} = \min\left(4.3\ A, \frac{V_{CC2}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}}\right)$$

where

- R_{ON} is the external turnon resistance.
- R_{GFET_Int} is the power transistor internal gate resistance, found in the power transistor data sheet.
- I_{OH} is the peak source current which is the minimum value between 4.3 A, the gate-driver peak source current, and the calculated value based on the gate-drive loop resistance. (1)

In this example, the peak source current is approximately 1.7 A as calculated in 公式 2.

$$I_{OH} = \frac{V_{CC2}}{R_{NMOS} \,||\, R_{OH} + R_{ON} + R_{GFET\_Int}} = \frac{20\ V}{4.5\ \Omega \,||\, 12\ \Omega + 2.2\ \Omega + 1.5\ \Omega} \approx 1.7\ A \quad (2)$$

Similarly, use 公式 3 to calculate the peak sink current.

$$I_{OL} = \min\left(4.4\ A, \frac{V_{CC2}}{R_{OL} + R_{OFF} + R_{GFET\_Int}}\right)$$

where

- R_{OFF} is the external turnoff resistance.
- I_{OL} is the peak sink current which is the minimum value between 4.4 A, the gate-driver peak sink current, and the calculated value based on the gate-drive loop resistance. (3)

In this example, the peak sink current is the minimum of 公式 4 and 4.4 A.

$$I_{OL} = \frac{V_{CC2}}{R_{OL} + R_{OFF} + R_{GFET\_Int}} = \frac{20\ V}{0.65\ \Omega + 0\ \Omega + 1.5\ \Omega} \approx 9.3\ A \quad (4)$$

注

The estimated peak current is also influenced by PCB layout and load capacitance. Parasitic inductance in the gate-driver loop can slow down the peak gate-drive current and introduce overshoot and undershoot. Therefore, TI strongly recommends that the gate-driver loop should be minimized. Conversely, the peak source and sink current is dominated by loop parasitics when the load capacitance (C_{ISS}) of the power transistor is very small (typically less than 1 nF) because the rising and falling time is too small and close to the parasitic ringing period.

10.2.2.3 Estimate Gate-Driver Power Loss

The total loss, P_G, in the gate-driver subsystem includes the power losses (P_{GD}) of the UCC53x0 device and the power losses in the peripheral circuitry, such as the external gate-drive resistor.

The P_{GD} value is the key power loss which determines the thermal safety-related limits of the UCC53x0 device, and it can be estimated by calculating losses from several components.

The first component is the static power loss, P_{GDQ}, which includes quiescent power loss on the driver as well as driver self-power consumption when operating with a certain switching frequency. The P_{GDQ} parameter is measured on the bench with no load connected to the OUT or OUTH and OUTL pins at a given V_{CC1}, V_{CC2}, switching frequency, and ambient temperature. In this example, V_{CC1} is 5 V and V_{CC2} is 20 V. The current on each power supply, with PWM switching from 0 V to 3.3 V at 1 kHz, is measured to be I_{CC1} = 1.67 mA and I_{CC2} = 1.11 mA. Therefore, use 公式 5 to calculate P_{GDQ}.

$$P_{GDO} = V_{CC1} \times I_{VCC1} + V_{CC2} \times I_{CC2} \approx 31\,mW \tag{5}$$

The second component is the switching operation loss, P_{GDO}, with a given load capacitance which the driver charges and discharges the load during each switching cycle. Use 公式 6 to calculate the total dynamic loss from load switching, P_{GSW}.

$$P_{GSW} = 2 \times V_{CC2} \times Q_G \times f_{SW}$$

where

- Q_G is the gate charge of the power transistor at V_{CC2}. (6)

If a split rail is used for turn-on and turnoff, then V_{CC2} is the total difference between the positive rail to the negative rail.

So, for this example application the total dynamic loss from load switching is approximately 4 mW as calculated in 公式 7.

$$P_{GSW} = 2 \times 20\ V \times 100\ nC \times 1\,kHz = 4\ mW \tag{7}$$

Q_G represents the total gate charge of the power transistor switching 400 V at 14 A, and is subject to change with different testing conditions. The UCC5320S gate-driver loss on the output stage, P_{GDO}, is part of P_{GSW}. P_{GDO} is equal to P_{GSW} if the external gate-driver resistance and power-transistor internal resistance are 0 Ω, and all the gate driver-loss will be dissipated inside the UCC5320S. If an external turnon and turnoff resistance exists, the total loss is distributed between the gate driver pullup and pulldown resistance, external gate resistance, and power-transistor internal resistance.

注

The pullup or pulldown resistance is a linear and fixed resistance if the source or sink current is not saturated to 4.3 A or 4.4 A (respectively), however, the resistance is nonlinear if the source or sink current is saturated. Therefore, P_{GDO} is different in these two cases as follows.

Use 公式 8 to calculate the linear pullup or pulldown resistor for case 1.

$$P_{GDO} = \frac{P_{GSW}}{2}\left(\frac{R_{OH} \,||\, R_{NMOS}}{R_{OH} \,||\, R_{NMOS} + R_{ON} + R_{GFET\_Int}} + \frac{R_{OL}}{R_{OL} + R_{OFF} + R_{GFET\_Int}}\right) \tag{8}$$

In this design example, all the predicted source and sink currents are less than 4.3 A and 4.4 A, therefore, use 公式 9 to estimate the UCC53x0 gate-driver loss.

$$P_{GDO} = \frac{4\ mW}{2}\left(\frac{12\ \Omega \,||\, 4.5\ \Omega}{12\ \Omega \,||\, 4.5\ \Omega + 2.2\ \Omega + 1.5\ \Omega} + \frac{0.65\ \Omega}{0.65\ \Omega + 0\ \Omega + 1.5\ \Omega}\right) \approx 1.5\ mW \quad (9)$$

Use 公式 10 to calculate the nonlinear pullup or pulldown resistor for case 2.

$$P_{GDO} = 2 \times f_{SW} \times \left[4.3\ A \times \int_0^{T_{R\_Sys}} \left(V_{CC2} - V_{OUTH}(t)\right)dt + 4.4\ A \times \int_0^{T_{F\_Sys}} V_{OUTL}(t)dt\right] \quad (10)$$

where

- $V_{OUTH/L(t)}$ is the gate-driver OUTH and OUTL pin voltage during the turnon and turnoff period. In cases where the output is saturated for some time, this value can be simplified as a constant-current source (4.3 A at turnon and 4.4 A at turnoff) charging or discharging a load capacitor. Then, the $V_{OUTH/L(t)}$ waveform will be linear and the T_{R_Sys} and T_{F_Sys} can be easily predicted.

For some scenarios, if only one of the pullup or pulldown circuits is saturated and another one is not, the P_{GDO} is a combination of case 1 and case 2, and the equations can be easily identified for the pullup and pulldown based on this discussion.

Use 公式 11 to calculate the total gate-driver loss dissipated in the UCC53x0 gate driver, P_{GD}.

$$P_{GD} = P_{GDQ} + P_{GDO} = 31\ mW + 1.5\ mW = 32.5\ mW \quad (11)$$

10.2.2.4 Estimating Junction Temperature

Use 公式 12 to estimate the junction temperature (T_J) of the UCC53x0 family.

$$T_J = T_C + \Psi_{JT} \times P_{GD} \quad (12)$$

where

- T_C is the UCC53x0 case-top temperature measured with a thermocouple or some other instrument.
- Ψ_{JT} is the junction-to-top characterization parameter from the Thermal Information table.

Using the junction-to-top characterization parameter (Ψ_{JT}) instead of the junction-to-case thermal resistance ($R_{\theta JC}$) can greatly improve the accuracy of the junction temperature estimation. The majority of the thermal energy of most ICs is released into the PCB through the package leads, whereas only a small percentage of the total energy is released through the top of the case (where thermocouple measurements are usually conducted). The $R_{\theta JC}$ resistance can only be used effectively when most of the thermal energy is released through the case, such as with metal packages or when a heat sink is applied to an IC package. In all other cases, use of $R_{\theta JC}$ will inaccurately estimate the true junction temperature. The Ψ_{JT} parameter is experimentally derived by assuming that the amount of energy leaving through the top of the IC will be similar in both the testing environment and the application environment. As long as the recommended layout guidelines are observed, junction temperature estimations can be made accurately to within a few degrees Celsius.

10.2.3 Selecting V_{CC1} and V_{CC2} Capacitors

Bypass capacitors for the V_{CC1} and V_{CC2} supplies are essential for achieving reliable performance. TI recommends choosing low-ESR and low-ESL, surface-mount, multi-layer ceramic capacitors (MLCC) with sufficient voltage ratings, temperature coefficients, and capacitance tolerances.

注

DC bias on some MLCCs will impact the actual capacitance value. For example, a 25-V, 1-μF X7R capacitor is measured to be only 500 nF when a DC bias of 15-V_{DC} is applied.

10.2.3.1 Selecting a V_{CC1} Capacitor

A bypass capacitor connected to the V_{CC1} pin supports the transient current required for the primary logic and the total current consumption, which is only a few milliamperes. Therefore, a 50-V MLCC with over 100 nF is recommended for this application. If the bias power-supply output is located a relatively long distance from the V_{CC1} pin, a tantalum or electrolytic capacitor with a value greater than 1 μF should be placed in parallel with the MLCC.

10.2.3.2 Selecting a V_{CC2} Capacitor

A 50-V, 10-µF MLCC and a 50-V, 0.22-µF MLCC are selected for the C_{VCC2} capacitor. If the bias power supply output is located a relatively long distance from the V_{CC2} pin, a tantalum or electrolytic capacitor with a value greater than 10 µF should be used in parallel with C_{VCC2}.

10.2.3.3 Application Circuits With Output Stage Negative Bias

When parasitic inductances are introduced by nonideal PCB layout and long package leads (such as TO-220 and TO-247 type packages), ringing in the gate-source drive voltage of the power transistor could occur during high di/dt and dv/dt switching. If the ringing is over the threshold voltage, unintended turnon and shoot-through could occur. Applying a negative bias on the gate drive is a popular way to keep such ringing below the threshold. A few examples of implementing negative gate-drive bias follow.

图 38 shows the first example with negative bias turnoff on the output using a Zener diode on the isolated power-supply output stage. The negative bias is set by the Zener diode voltage. If the isolated power supply is equal to 25 V, the turnoff voltage is –5.1 V and the turnon voltage is 25 V – 5.1 V ≈ 20 V.

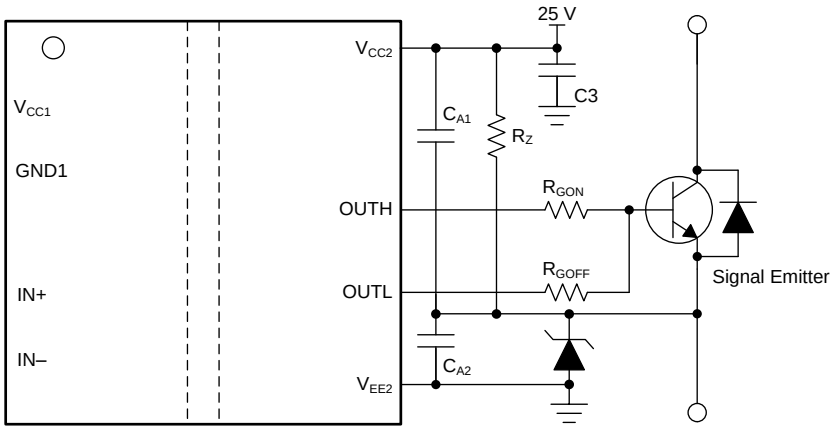


图 38. Negative Bias With Zener Diode on Iso-Bias Power-Supply Output (UCC5320S and UCC5390S)

图 39 shows another example which uses two supplies (or single-input, double-output power supply). The power supply across V_{CC2} and GND2 determines the positive drive output voltage and the power supply across V_{EE2} and GND2 determines the negative turnoff voltage. This solution requires more power supplies than the first example, however, it provides more flexibility when setting the positive and negative rail voltages.

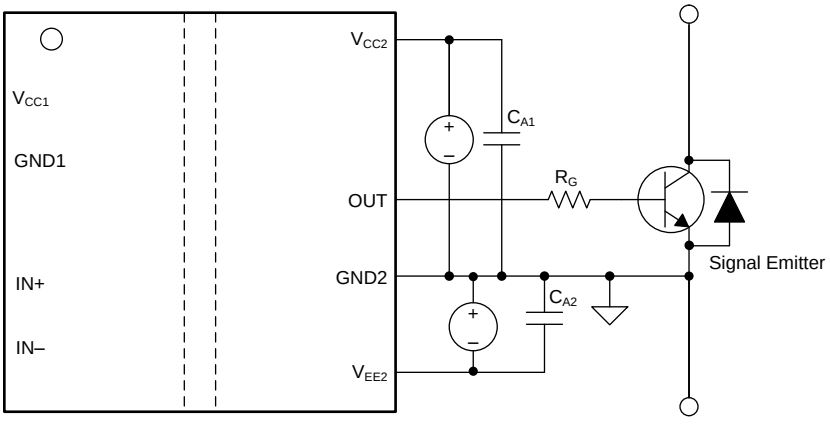
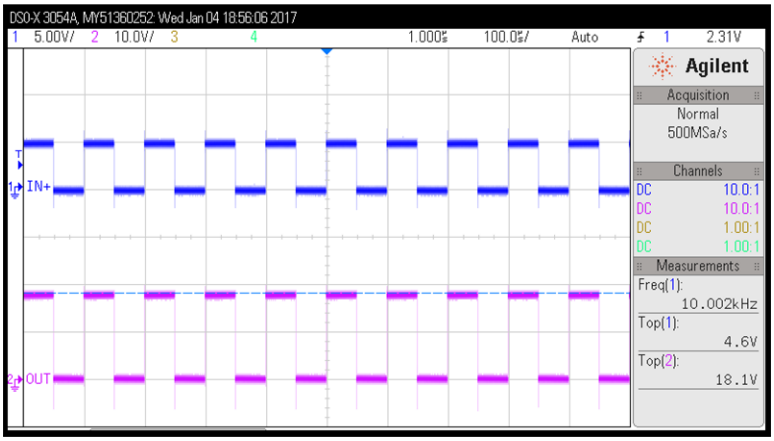


图 39. Negative Bias With Two Iso-Bias Power Supplies (UCC5320E and UCC5390E)

10.2.4 Application Curve



V_{CC2} = 20 V V_{EE2} = GND f_{SW} = 10 kHz

图 40. PWM Input And Gate Voltage Waveform

11 Power Supply Recommendations

The recommended input supply voltage (V_{CC1}) for the UCC53x0 device is from 3 V to 15 V. The lower limit of the range of output bias-supply voltage (V_{CC2}) is determined by the internal UVLO protection feature of the device. The V_{CC1} and V_{CC2} voltages should not fall below their respective UVLO thresholds for normal operation, or else the gate-driver outputs can become clamped low for more than 50 µs by the UVLO protection feature. For more information on UVLO, see the *Undervoltage Lockout (UVLO)* section. The higher limit of the V_{CC2} range depends on the maximum gate voltage of the power device that is driven by the UCC53x0 device, and should not exceed the recommended maximum V_{CC2} of 33 V. A local bypass capacitor should be placed between the V_{CC2} and V_{EE2} pins, with a value of 220-nF to 10-µF for device biasing. TI recommends placing an additional 100-nF capacitor in parallel with the device biasing capacitor for high frequency filtering. Both capacitors should be positioned as close to the device as possible. Low-ESR, ceramic surface-mount capacitors are recommended. Similarly, a bypass capacitor should also be placed between the V_{CC1} and GND1 pins. Given the small amount of current drawn by the logic circuitry within the input side of the UCC53x0 device, this bypass capacitor has a minimum recommended value of 100 nF.

If only a single, primary-side power supply is available in an application, isolated power can be generated for the secondary side with the help of a transformer driver such as Texas Instruments' SN6501 or SN6505A. For such applications, detailed power supply design and transformer selection recommendations are available in *SN6501 Transformer Driver for Isolated Power Supplies* data sheet and *SN6505A Low-Noise 1-A Transformer Drivers for Isolated Power Supplies* data sheet.

12 Layout

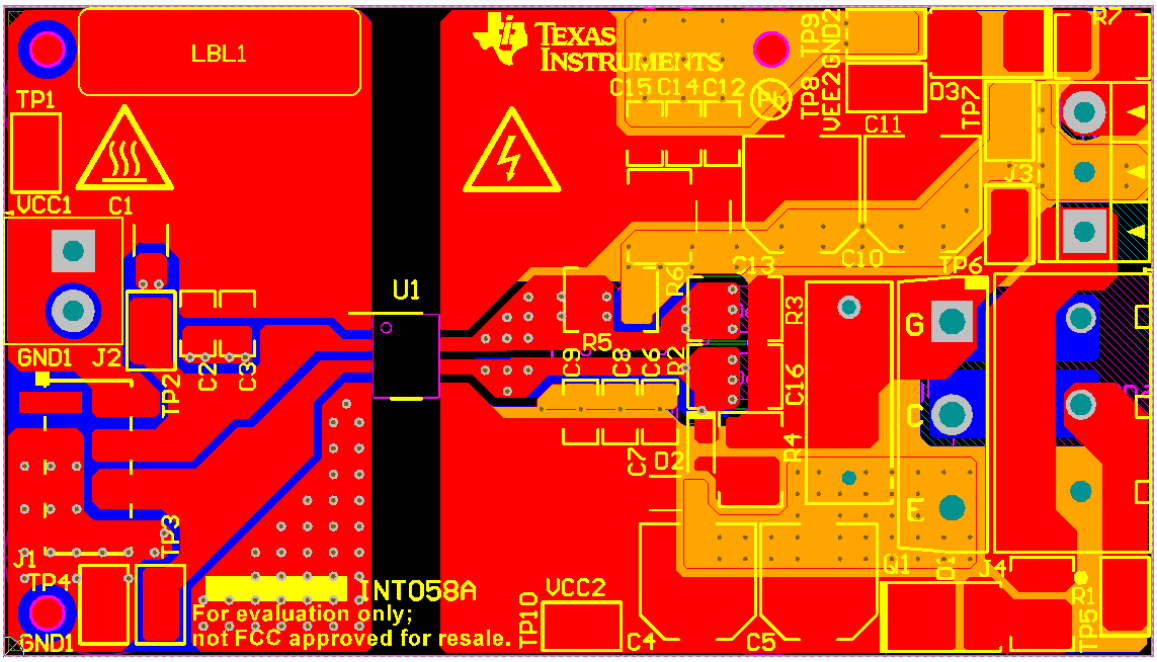
12.1 Layout Guidelines

Designers must pay close attention to PCB layout to achieve optimum performance for the UCC53x0. Some key guidelines are:

- Component placement:
  - Low-ESR and low-ESL capacitors must be connected close to the device between the V_{CC1} and GND1 pins and between the V_{CC2} and V_{EE2} pins to bypass noise and to support high peak currents when turning on the external power transistor.
  - To avoid large negative transients on the V_{EE2} pins connected to the switch node, the parasitic inductances between the source of the top transistor and the source of the bottom transistor must be minimized.
- Grounding considerations:
  - Limiting the high peak currents that charge and discharge the transistor gates to a minimal physical area is essential. This limitation decreases the loop inductance and minimizes noise on the gate terminals of the transistors. The gate driver must be placed as close as possible to the transistors.
- High-voltage considerations:
  - To ensure isolation performance between the primary and secondary side, avoid placing any PCB traces or copper below the driver device. PCB cutting or scoring beneath the IC are not recommended because this can severely exacerbate board warping and twisting issues.
- Thermal considerations:
  - A large amount of power may be dissipated by the UCC53x0 if the driving voltage is high, the load is heavy, or the switching frequency is high (for more information, see the *Estimate Gate-Driver Power Loss* section). Proper PCB layout can help dissipate heat from the device to the PCB and minimize junction-to-board thermal impedance (θ_{JB}).
  - Increasing the PCB copper connecting to the V_{CC2}, GND1, and V_{EE2} pins is recommended, with priority on maximizing the connection to V_{EE2}. However, the previously mentioned high-voltage PCB considerations must be maintained.
  - If the system has multiple layers, TI also recommends connecting the V_{CC2} and V_{EE2} pins to internal ground or power planes through multiple vias of adequate size. These vias should be located close to the IC pins to maximize thermal conductivity. However, keep in mind that no traces or coppers from different high voltage planes are overlapping.

12.2 Layout Example

图 41 shows a PCB layout example with the signals and key components labeled.



(1) No PCB traces or copper are located between the primary and secondary side, which ensures isolation performance.

图 41. Layout Example

Layout Example (接下页)

图 42 and 图 43 show the top and bottom layer traces and copper.

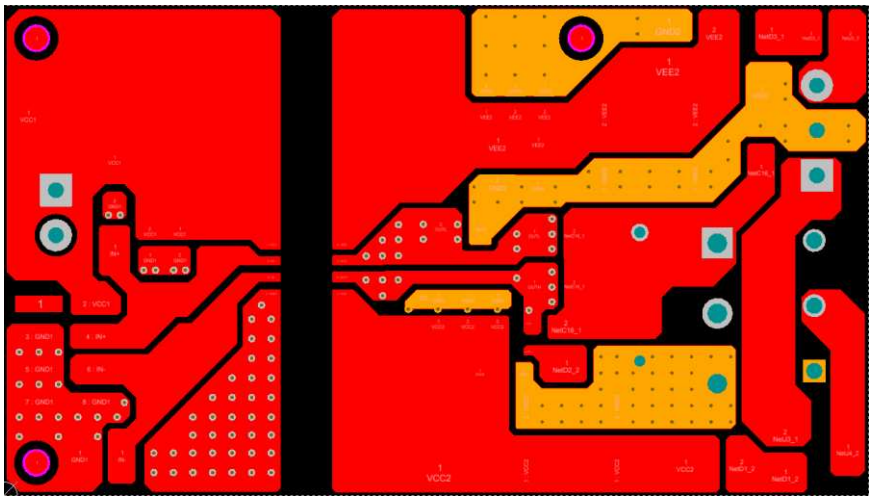


图 42. Top-Layer Traces and Copper

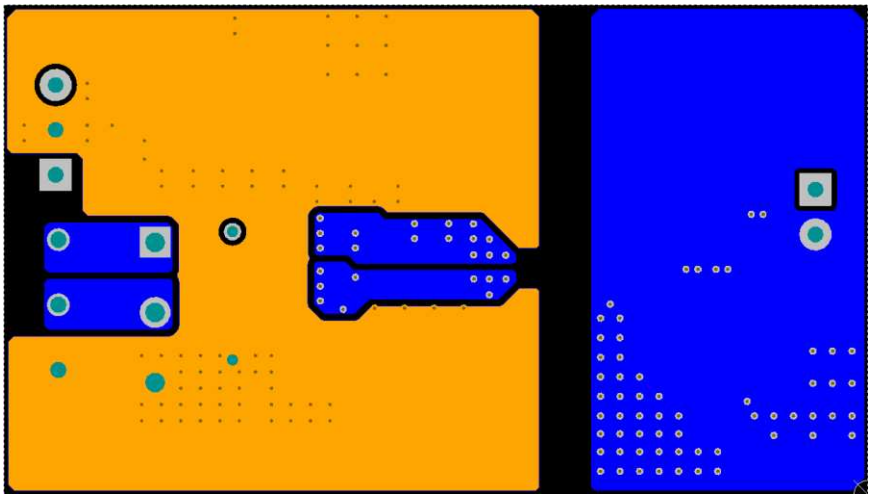
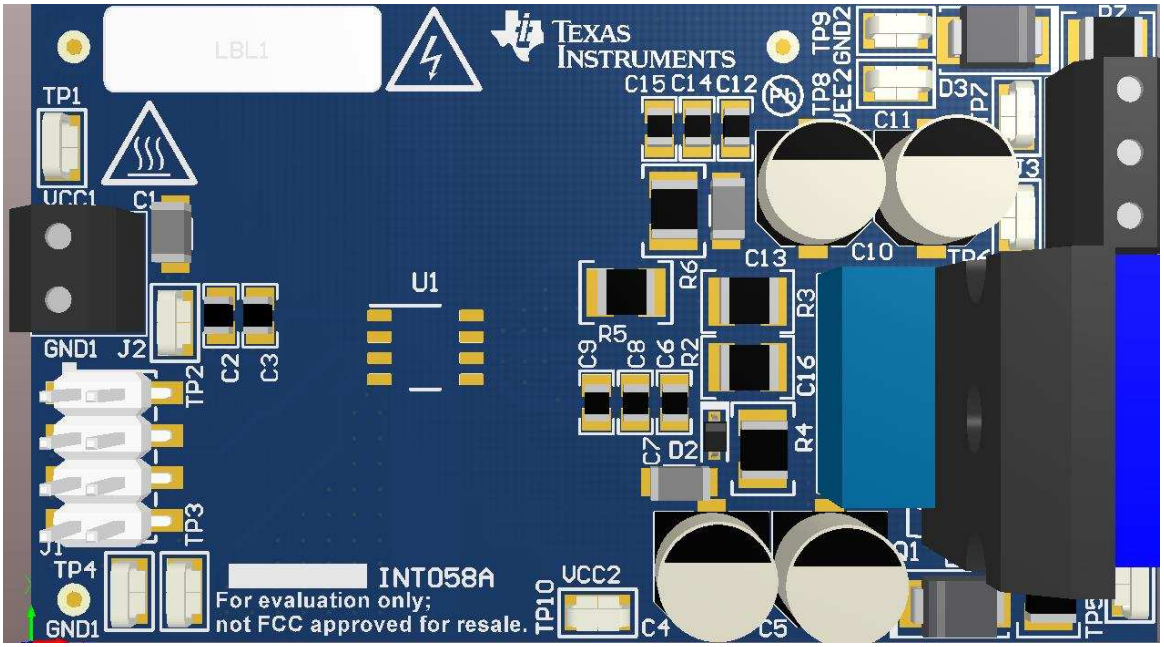


图 43. Bottom-Layer Traces and Copper (Flipped)

Layout Example (接下页)

图 44 shows the 3D layout of the top view of the PCB.



(1) The location of the PCB cutout between primary side and secondary sides ensures isolation performance.

图 44. 3-D PCB View

12.3 PCB Material

Use standard FR-4 UL94V-0 printed circuit board. This PCB is preferred over cheaper alternatives because of lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and the self-extinguishing flammability-characteristics.

图 45 shows the recommended layer stack.

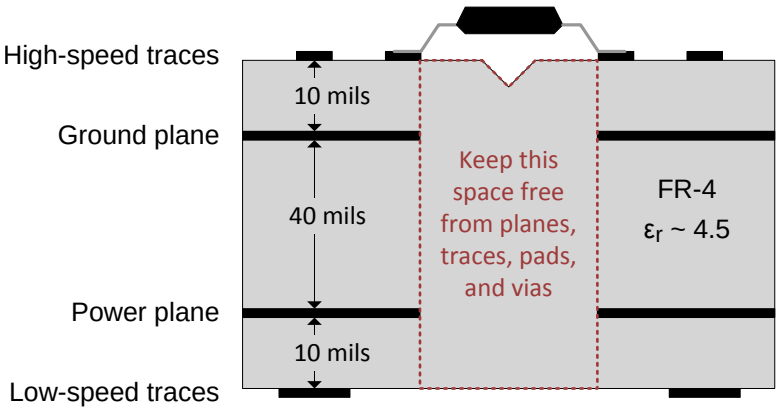


图 45. Recommended Layer Stack

13 器件和文档支持

13.1 文档支持

13.1.1 相关文档

请参阅如下相关文档：

- 德州仪器 (TI)，*数字隔离器设计指南*
- 德州仪器 (TI)，*隔离相关术语*
- 德州仪器 (TI)，*《SN6501 用于隔离式电源的变压器驱动器》数据表*
- 德州仪器 (TI)，*《SN6505A 用于隔离式电源的低噪声 1A 变压器驱动器》数据表*
- 德州仪器 (TI)，*UCC53x0xD 评估模块用户指南*

13.2 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

表 **6.** 相关链接

器件	产品文件夹	立即订购	技术文档	工具和软件	支持和社区
UCC5310	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UCC5320	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UCC5350	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
UCC5390	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

13.3 接收文档更新通知

要接收文档更新通知，请导航至德州仪器 TI.com.cn 上的器件产品文件夹。请单击右上角的*通知我* 进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

13.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 在线社区 ***TI 的工程师对工程师 (E2E) 社区。*** **此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。**

设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

13.5 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

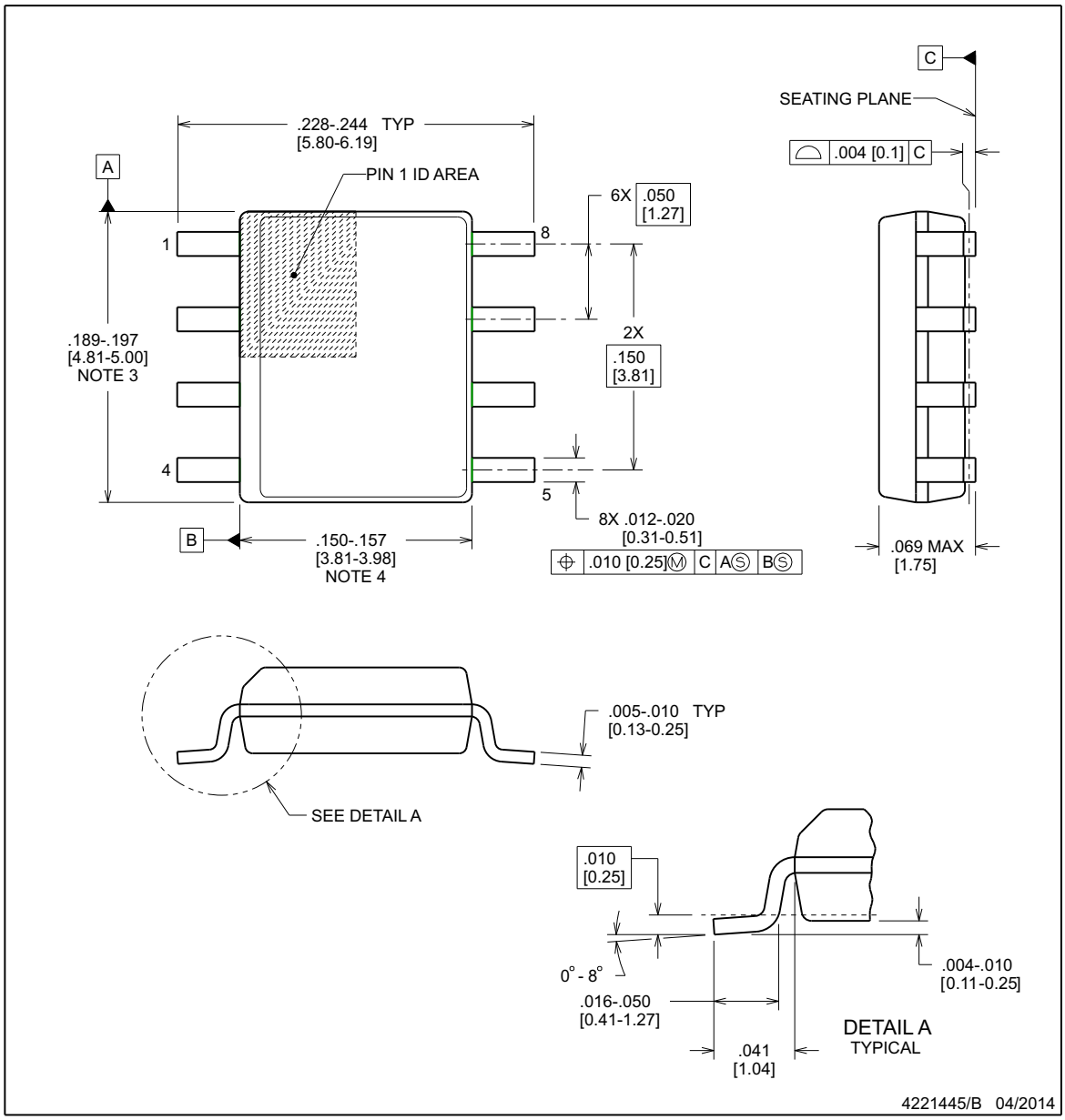
以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航栏。

PACKAGE OUTLINE

D0008B

SOIC - 1.75 mm max height

SOIC



NOTES:

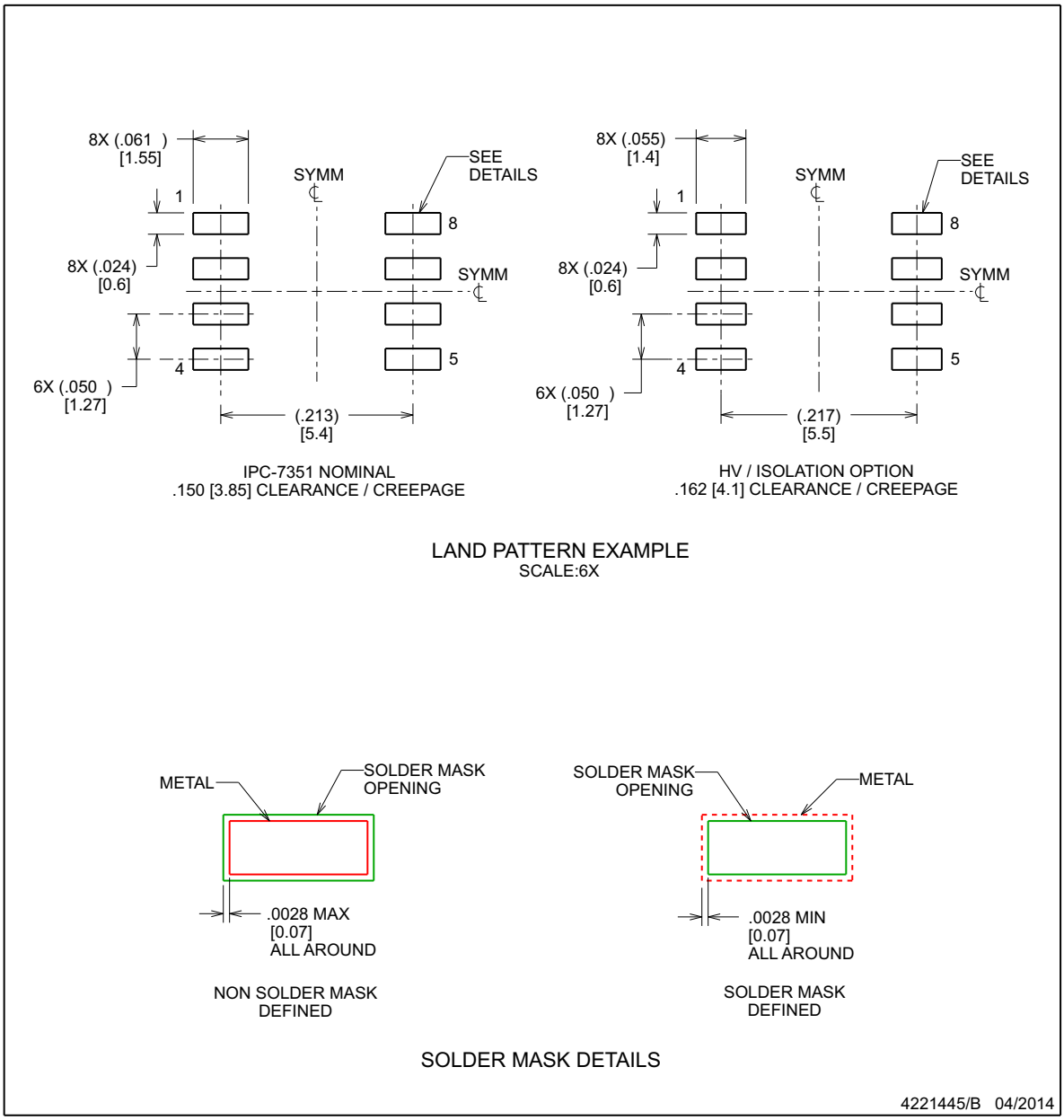
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15], per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008B

SOIC - 1.75 mm max height

SOIC



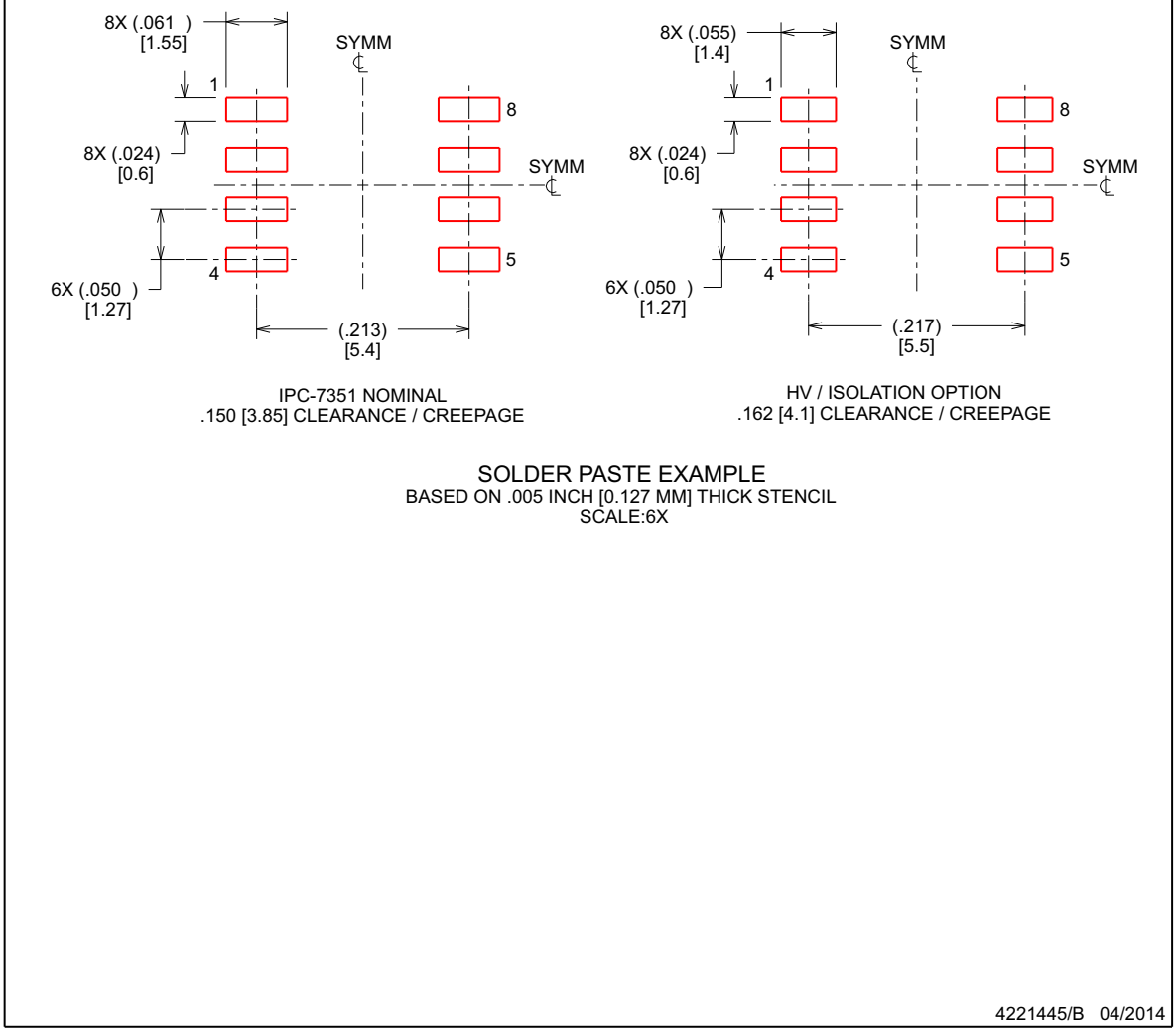
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008B — **SOIC - 1.75 mm max height**

SOIC



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC5310MCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5310M	Samples
UCC5310MCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5310M	Samples
UCC5320ECD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5320E	Samples
UCC5320ECDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5320E	Samples
UCC5320SCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5320S	Samples
UCC5320SCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5320S	Samples
UCC5350MCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5350M	Samples
UCC5350MCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	5350M	Samples
UCC5390ECD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53X0E	Samples
UCC5390ECDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53X0E	Samples
UCC5390SCD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53X0S	Samples
UCC5390SCDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	53X0S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

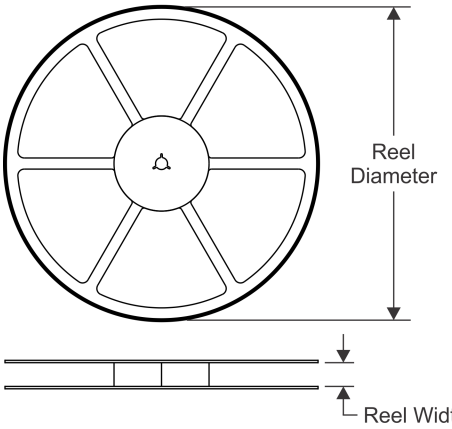
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

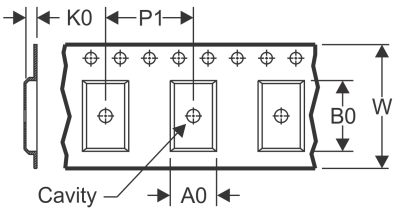
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

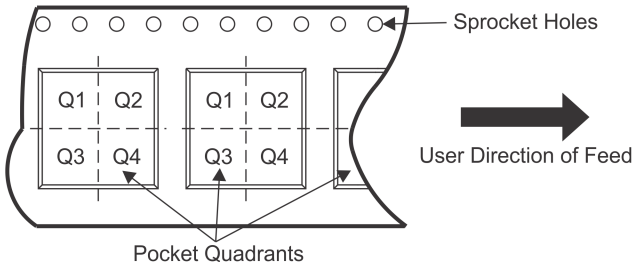


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

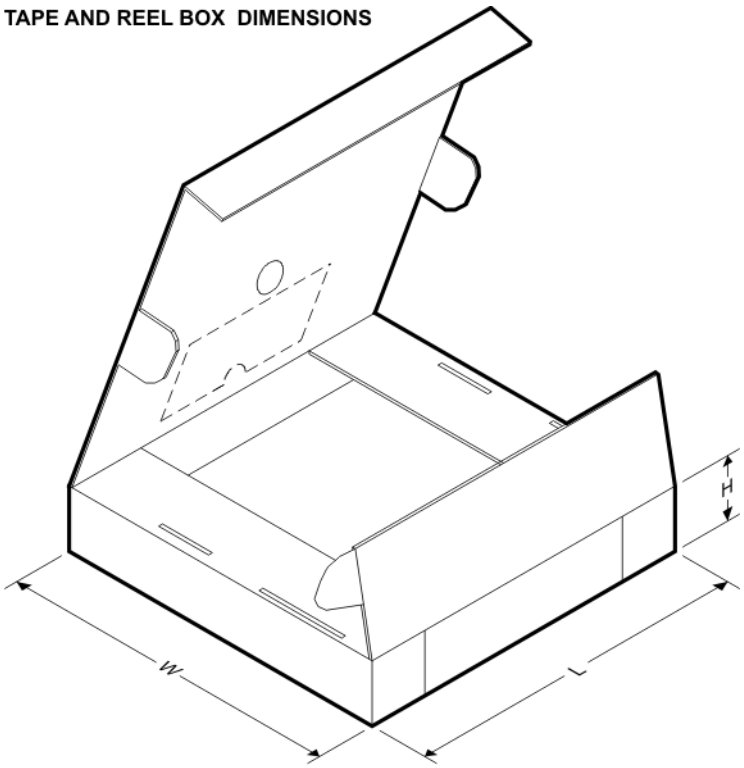
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC5310MCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC5320ECDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC5320SCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC5350MCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC5390ECDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC5390SCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

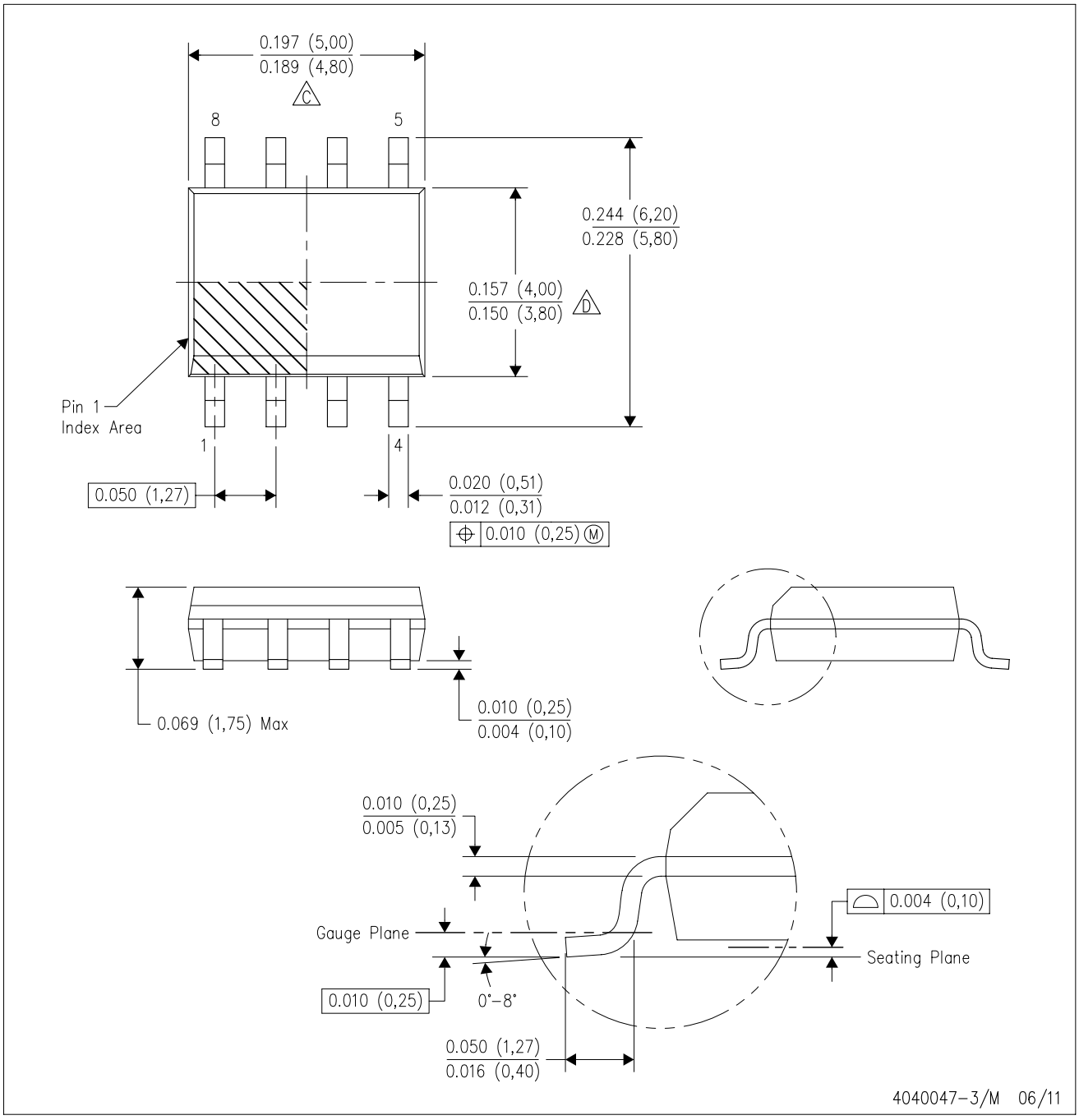
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC5310MCDR	SOIC	D	8	2500	367.0	367.0	38.0
UCC5320ECDR	SOIC	D	8	2500	367.0	367.0	38.0
UCC5320SCDR	SOIC	D	8	2500	367.0	367.0	38.0
UCC5350MCDR	SOIC	D	8	2500	367.0	367.0	38.0
UCC5390ECDR	SOIC	D	8	2500	367.0	367.0	38.0
UCC5390SCDR	SOIC	D	8	2500	367.0	367.0	38.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

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